Design considerations for CMOS low-noise amplifiers

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Design Considerations for CMOS Low-Noise Amplifiers[1]

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Abstract — **A low-noise amplifier is the first active stage of a CMOS RF receiver. The inductively degenerated common-source LNA (CS-LNA) topology is currently popular because it achieves high gain, low noise figure, etc. In this paper, its performance is reviewed and the optimum Q value that gives minimum noise figure is derived. It is then compared to the conventional common-gate LNA (CG-LNA) in terms of gain, noise figure, input matching, reverse isolation and stability. Finally, a general g_m-boosted design technique for common-gate RF circuits is introduced that provides lower noise figure and power consumption than the conventional CS-LNA and CG-LNA stages; it also preserves the CG-LNA insensitivity to parasitic input capacitances. In view of CMOS scaling, the CG-LNA topology is attractive for future higher frequency and/or lower power designs.**

Index Terms — **Low-noise amplifier, noise figure, RF receiver.**

I. Introduction

Wireless communications systems demand high levels of integration, complex functionalities, and low cost implementations. After more than a decade of intensive research, CMOS has emerged as a viable technology for mixed-signal/RF system-on-chip solutions owing to the continued scaling of channel lengths; i.e., Moore's Law.

In an RF receiver, the input signal from an antenna first passes through an LNA that amplifies it and suppresses noise contributions from subsequent stages [1]. Hence, low noise figure and high gain are critical LNA performance parameters; in portable applications, low power dissipation is also essential. LNA design involves tradeoffs among linearity, input matching, power dissipation, etc.

The basic common-source and common-gate LNA circuits depicted in Fig. 1 are widely used in CMOS RF IC design. The CS-LNA configuration is currently popular because of its superior noise performance; i.e., the inductive degeneration is ideally noiseless and the RF input signal is pre-amplified by the input-matching series resonant network. In contrast, the CG-LNA topology provides a wideband input match that is less sensitive to input parasitic capacitances (e.g., bond pad, etc.) [2].

In this paper, a general g_m-boosted design technique for common-gate RF circuits is presented. Implemented using cross-coupled capacitors, a fully differential g_m-boosted CG-LNA exhibits superior performance to its conventional common-gate counterpart and outperforms the CS-LNA configuration at higher RF frequencies. (Note: Although not described herein, implementations of the g_m-boosted technique are also possible using other passive coupling networks such as inductors, etc.) The paper is organized as follows: Section II compares the basic CS-LNA and CG-LNA topologies in terms of gain, noise figure, input matching accuracy, etc. Section III describes the general g_m-boosted technique and presents results that confirm its advantages. Conclusions are given in Section IV.

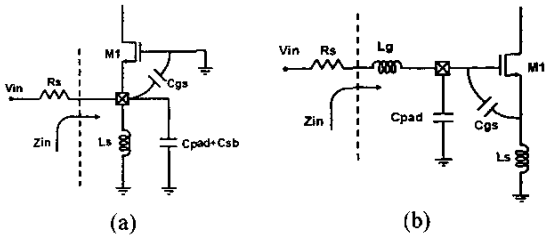

Fig. 1. Basic low-noise amplifier topologies: (a) Common-gate (CG-LNA), and (b) common-source (CS-LNA).

II. CMOS LNA Topologies

A task in LNA design is to create a 50Ω resistive input impedance as required by the preceding band-select filter. Its key specifications including insertion loss, pass band ripple, stop band attenuation, etc., are guaranteed to be met only over a specified range of terminating impedances; e.g., between 25Ω and 100Ω. Terminating impedances outside this range result in substantial performance degradations. The LNA should also be designed so that it adds minimum noise in the RF signal path while synthesizing the input impedance of 50Ω. This precludes obvious approaches such as shunting a 50Ω resistor at the input to create the termination impedance. Next, performance characteristics of the basic CS-LNA and CG-LNA topologies are analyzed and compared.

A. Input Matching

The input impedance (50Ω) of the CG-LNA stage (Fig. 1(a)) is approximately $1/g_{m1}$ of input MOSFET M_1, while that of the CS-LNA circuit (Fig. 1(b)) is [3]:

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$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \left(\frac{g_{m1}}{C_{gs}}\right)L_s$$
$$\approx s(L_g + L_s) + \frac{1}{sC_{gs}} + \omega_T L_s$$

Z_{in} is specified by choosing L_g and L_s to resonate with C_{gs} at the operating frequency with $(g_{m1}/C_{gs})L_s$ set to 50Ω.

A fundamental difference between the input matching networks is that CS-LNA is series resonant while CG-LNA is parallel resonant; the associated quality factors are

$$Q_{CS-LNA} = \frac{1}{2\omega_0 C_{gs} R_s} > 1 \leftrightarrow Q_{CG-LNA} = \frac{\omega_0 C_{gs} R_s}{2} < 1$$

It is known that the sensitivity of Z_{in} to parasitic components is proportional to the quality factor of the matching network [4]. Hence, CG-LNA with its lower Q parallel resonant network is more robust against typical production process, voltage, and temperature variations. Moreover, parasitic capacitance at the CG-LNA input is naturally absorbed into the LC tank (Fig. 1(a)).

B. Gain

The effective transconductance of the CS-LNA stage is

$$G_{m,CS-LNA} = g_{m1}Q = \frac{g_{m1}}{\omega_0 C_{gs}(R_S + \omega_T L_s)} = \frac{\omega_T}{\omega_0 R_S\left(1 + \frac{\omega_T L_s}{R_S}\right)}$$

With the input matched to R_S,

$$G_{m,CS-LNA} = \frac{1}{2R_S}\left(\frac{\omega_T}{\omega_0}\right)$$

In RF systems R_S is usually equal to 50Ω. Note that G_m depends only on the ratio of ω_T to ω_0 and is independent of the MOSFET small-signal transconductance g_{m1}. In contrast, the effective input transconductance of CG-LNA under perfect input matching conditions is

$$G_{m,CG-LNA} = \frac{1}{2}g_{m1} = \frac{1}{2R_S}$$

The value of ω_T/ω_0 typically lies in the range of 5~10, depending on the operating frequency and process details. Therefore, CS-LNA provides higher gain than its conventional common-gate counterpart.

C. Noise Figure

A major advantage of the common-source amplifier with inductive degeneration is that the resistive input impedance is noiseless, unlike other topologies where a noisy resistor is added in the signal path to create a 50Ω terminating impedance. Figure 2 depicts a small-signal circuit for noise analysis of CS-LNA with inductive degeneration. The noise factor of this topology is

$$F = \frac{\overline{i_{n,out}^2}}{\overline{i_{Rs}^2}} = 1 + \frac{\gamma}{\alpha}\frac{1}{Q}\left(\frac{\omega_0}{\omega_T}\right)\left[1 + \frac{\delta\alpha^2}{5\gamma}(1+Q^2) + 2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right] \quad (1)$$

$$\overline{i_{Rs}^2} = \frac{4kT\Delta f}{R_s}$$
$$\overline{i_d^2} = 4kT\gamma\, g_{d0}\Delta f$$
$$\overline{i_g^2} = 4kT\delta\, g_g \Delta f$$
$$Q = \frac{1}{\omega_0 C_{gs} R_s}$$
$$\overline{i_g i_d^*} = c\sqrt{\overline{i_g^2}\,\overline{i_d^2}}$$

where c = $j0.395$, α, γ, and δ are bias-dependent parameters [5], and ω_0 and ω_T are the operating and unity current gain frequencies, respectively.

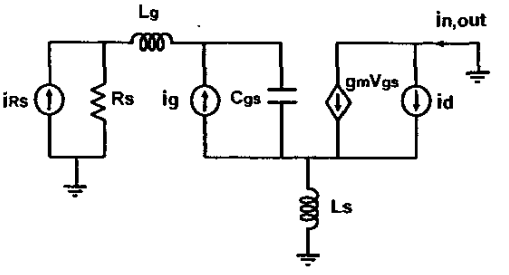

Fig. 2. Small-signal circuit for noise figure analysis of CS-LNA.

The results above reveal the impact of Q on noise figure in CS-LNA. From (1), noise in CS-LNA comprises three factors: channel noise, gate noise and correlated noise. Increasing Q of the input resonant circuit reduces the contribution of channel noise. In contrast, gate noise is enhanced by the Q factor. Hence, there exists an optimum Q that minimizes the noise figure. For a given overdrive voltage and f_T, the optimum values are

$$F_{\min,CS-LNA} = 1 + \frac{\gamma}{\alpha}\left(\frac{\omega_0}{\omega_T}\right)\frac{2\delta\alpha^2}{5\gamma}Q_{opt} \quad (2)$$
$$Q_{opt} = \sqrt{1 + 2|c|\sqrt{\frac{5\gamma}{\delta\alpha^2}} + \frac{5\gamma}{\delta\alpha^2}}$$

To achieve a high f_T, minimum channel length is used. Knowing the optimum Q value for minimum noise figure, the optimum width of the device is then easily determined.

For CG-LNA, the noise factor is approximately constant with respect to the operating frequency,

$$F_{CG-LNA} = 1 + \frac{\gamma}{\alpha}$$

The noise factor of CG-LNA is constant with respect to ω_0/ω_T, while that of CS-LNA is linear with ω_0/ω_T.

D. Reverse Isolation and Stability

In a conventional CS-LNA, C_{gd} provides a feed-forward path between input and output that degrades reverse isolation and stability. In contrast, since the Miller effect on C_{gd} does not exist in CG-LNA; it exhibits better reverse isolation and stability. Also, cascoding is not necessary in

conventional CG-LNA so there is no added noise from cascode transistors.

In summary, CG-LNA achieves better input matching, reverse isolation and stability than CS-LNA. However, the higher noise figure has impeded its use for low noise amplification. In the next section, it is shown that the g_m-boosted technique is advantageous in common-gate amplifiers to achieve a lower noise figure, especially at higher frequencies, while consuming less power.

III. G_m-Boosted CG-LNA Topology

Since noise figure is the most important characteristic of an LNA, the noise calculations of the CG-LNA stage are briefly revisited. It can be shown that the noise factor is

$$F_{CG-LNA} = 1 + \frac{\gamma}{\alpha} \frac{1}{g_{m1} R_S} \tag{3}$$

where induced gate noise is negligibly small.

As (3) implies, increasing g_{m1} reduces the noise factor. In RF systems, however, input matching requires that $g_{m1} = 1/R_S$, which results in $F = 1+\gamma/\alpha$. From another point of view, it is the input-matching requirement that prevents increasing g_{m1} to lower the noise factor, and this in turn sets a lower bound on the noise factor. Note that in CG-LNA, impedance matching may be traded against noise figure. More specifically, if some input mismatch can be tolerated, g_{m1} can be increased to decrease the noise figure while the input reflection is maintained below some reasonable value [2]. For example, if $\gamma = 2$ and $1/g_{m1} = 30\Omega$, $S_{11} = -12$dB, which is often acceptable. In this case, NF = 3.4dB, which is about 1.4dB lower than the value of 4.8dB when the input is matched to 50Ω.

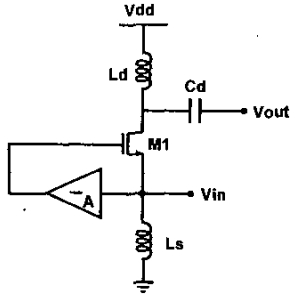

Fig. 3. G_m-boosted common-gate LNA.

The discussion above illuminates the tight link between noise figure and input matching in CG-LNA. If the condition of input matching can be separated from noise performance, the possibility of improving noise figure arises. The proposed scheme is based on an important observation: two g_m values are used in calculating the noise factor of the common-gate amplifier. One is the effective transconductance looking into the source terminal; denote it as G_m. The other is the intrinsic transconductance of the amplifying device, which is related to drain current channel noise i_d and is denoted as g_{m1}. In general, G_m is not necessarily equal to g_{m1}. However, in a conventional CG-LNA in which the gate terminal is shorted to ac ground, $G_m = g_{m1}$. A design challenge in improving CG-LNA is to modify the topology so that $G_m \neq g_{m1}$. Specifically, to make $G_m \neq g_{m1}$, a coupling mechanism is introduced between the gate and source terminals.

Figure 3 depicts the topology of the proposed g_m-boosted CG-LNA. In this structure, rather than connecting the gate terminal to a dc bias voltage, an inverting amplification is introduced between the source and gate nodes of the MOSFET. Consequently, the effective transconductance looking into the source terminal is boosted from $G_m = g_{m1}$ to $G_m = (1+A)g_{m1}$, where A is the gain from source to gate. Most important, the resulting noise factor becomes

$$F_{CG-LNA,GM-BOOSTED} = 1 + \frac{\gamma}{\alpha} \frac{1}{(1+A)^2 g_{m1} R_S}$$

Input matching requires that $(1+A)g_{m1} = 1/R_S$ resulting in

$$F_{CG-LNA,GM-BOOSTED} = 1 + \frac{\gamma}{\alpha} \frac{1}{1+A}$$

It is clear that the noise factor of the structure shown in Fig. 3 is reduced by the factor (1+A). For example, if A=1, γ=2, δ=4, α=0.85, then

$$NF_{CG-LNA} = 5.25dB \leftrightarrow NF_{CG-LNA,GM-BOOSTED} = 3.38dB$$

It can be seen that 1.9dB of improvement in the noise figure is achieved by the g_m-boosted CG-LNA relative to its conventional counterpart.

Figure 4 compares noise figures of various LNA circuits. The g_m-boosted CG-LNA (with A = 1) achieves lower noise figure than CS-LNA for $\omega_0/\omega_T > 0.35$. In addition, if $1/g_m = 30\Omega$, $S_{11} = -12$dB, which is usually an acceptable value, the g_m-boosted CG-LNA outperforms CS-LNA for $\omega_0/\omega_T > 0.2$. It also consumes less power than the conventional CG-LNA. That is, since $(1+A)g_{m,new} = 1/R_S$, $g_{m,new}$ is reduced to $1/(1+A)g_m$ and the power consumption is reduced by the same factor. The g_m-boosted CG-LNA is attractive for high frequency applications.

Next, capacitor cross-coupled CG-LNA [6] is reviewed as one possible implementation of a g_m-boosted CG-LNA. As shown in Fig. 3, an inverting amplification is required between the source and gate terminals. In differential circuits, the inverting gain is naturally available (with A = 1) as shown in Fig. 5 wherein L_s resonates with the input

node capacitance at the operating frequency. L_d and C_d form an L-match circuit at the output. However, unlike in conventional CG-LNA, C_{gd} in Fig. 5 experiences the Miller effect, which degrades the reverse isolation. Cascodes (M_3 and M_4) are added to improve reverse isolation and stability.

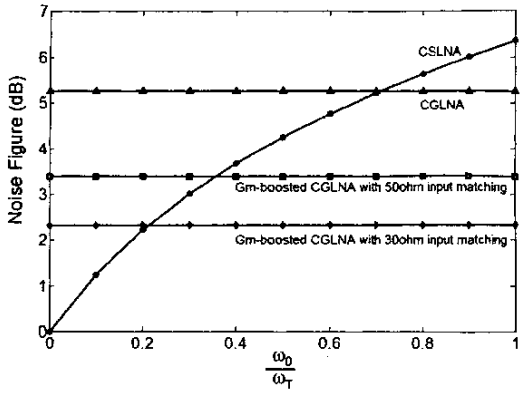

Fig. 4. Noise figure of the CS-LNA, CG-LNA and g_m-boosted CG-LNA stages versus ω_0/ω_T.

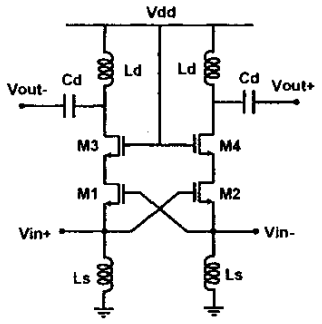

Fig. 5. Capacitor cross-coupled common-gate LNA [6].

The circuit of Fig. 5 is simulated in *SPECTRE-RF* at 5.6GHz. The simulations are performed using a 1.8V, 180nm CMOS technology. For comparison, the conventional CS-LNA and CG-LNA shown in Fig. 1 are also designed and simulated using the same process. Table I compares the performance of conventional CS-LNA, CG-LNA and capacitive cross-coupling CG-LNA circuits. Simulation results show that the capacitive cross-coupling CG-LNA circuit achieves a lower noise figure and consumes less dc power. Furthermore, the calculated noise figure for the capacitor cross-coupled CG-LNA based on the analysis described above for g_m-boosted CG-LNA agrees closely with the simulated results.

Table I. LNA Performance Comparison

	CS-LNA	CG-LNA	Gm-Boosted CG-LNA
Frequency (GHz)	5.6	5.6	5.6
S11 (dB)	-28.1	-39.6	-16.4
S21 (dB)	16.2	9.0	10.4
S12 (dB)	-28.3	-40.7	-44.3
S22 (dB)	-23.4	-25.6	-26.4
NF (dB)	2.87	2.95	1.69
NF with M_1 only (dB)	2.26	2.10	1.00
Calculated NF (dB)	NA	2.08	0.95
IIP3 (dBm)	-5.1	3.64	2.96
DC Current (mA)	6.2	2.65	1.80×2

IV. Conclusions

A general g_m-boosted CG-LNA topology is detailed that exhibits lower noise figure and consumes less power than conventional CG-LNA. It also preserves the advantages of insensitivity to parasitic input capacitance, higher reverse isolation and better stability, which makes it attractive for emerging high frequency applications. Implementation of the g_m-boosted CG-LNA scheme is also discussed and simulations show good agreement between analysis and simulated results. The g_m-boosted topology provides new opportunities for circuit innovation; implementations using other coupling techniques are under development.

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29.3 Low-Power g_m-boosted LNA and VCO Circuits in 0.18μm CMOS

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As multi-channel transceivers emerge, there is a growing demand for CMOS RF front-end circuits that give state-of-the-art performance, consume less power, and exhibit robustness against PVT variations. Previously, the inductively degenerated common-source LNA (CSLNA) and the cross-coupled LC VCO topologies were dominant. We propose the passively-coupled common-gate LNA (CGLNA) and Colpitts VCO configurations as alternatives. A CGLNA, a differential Colpitts VCO, and a quadrature VCO (QVCO) are presented that employ g_m-boosting with low current consumption.

A conventional CGLNA (Fig. 29.3.1a) has superior input matching, linearity, stability and robustness to PVT variations [1], but the inductively degenerated CSLNA achieves a lower noise figure (NF) at low operating frequencies. The input matching requirement of g_mR_s=1 for CGLNA bounds its noise factor at $F = 1+\gamma/\alpha$ where $\alpha = g_m/g_{d0}$. Clearly, α should be increased to decrease F. This seems infeasible because α is constrained at the device level. However, passive coupling techniques proposed herein allow the *effective* g_m to be increased without increasing g_{d0}. Figure 29.3.1b depicts the g_m-boosted scheme where an inverting gain from source to gate decouples g_m from g_{d0}. The effective transconductance at the input is increased to $(1+A)g_m$ and F is reduced to $1+\gamma/(1+A)\alpha$.

Noise issues prohibit active realizations of the inverting gain A. One possible passive implementation employs capacitor cross-coupling using inversions available in a differential topology [2]. However, a differential configuration consumes 2X more current and silicon area than a single-ended version, and the gate capacitance makes A<1.

To minimize current consumption and realize A≥1, an on-chip transformer is used to achieve anti-phase operation between the source and gate terminals of M_1 (Fig. 29.3.1c). $A = kn = k\sqrt{L_s/L_p}$ is determined by the turns ratio n and the coupling factor k of transformer T_1. The small-signal input admittance at the source is $Y_{in} \approx 1/sL_p+(1+kn)g_m+(1+2kn+n^2)sC_{gs}$. Assuming ideal magnetic coupling (k=1) and n=1:1, $Y_{in} \approx 1/sL_p+2g_m+4sC_{gs}$. Thus, the use of transformer coupling effectively doubles the transconductance and enables a 2X reduction in power consumption. In addition, F is reduced to $1+\gamma/2\alpha$ under the new input matching condition $2g_mR_s$=1.

LNA and VCO circuits share many similarities. For example, a Colpitts oscillator can be viewed as a common-gate amplifier in a positive feedback configuration. Its phase noise is superior to a cross-coupled VCO [3] because the noise current from active devices is injected into the *LC* tank when the tank voltage is minimum and the impulse sensitivity is low. However, poor start-up characteristics, high power consumption, lower tuning range and lack of differential operation have impeded its adoption. The design presented in [3] addresses these shortcomings through the use of a current-switching technique. We use the common-gate g_m-boosting techniques to overcome these drawbacks.

In order to realize a differential Colpitts oscillator with enhanced transconductance, the gate of one branch is connected to a node with an opposite voltage swing to that of the source. As depicted in Fig. 29.3.2a, the two branches can be capacitive cross-coupled. The resultant increase in transconductance eases the start-up requirement with lower power consumption than other techniques. The in-phase relationship between the source and drain voltages (via capacitive feedback with C_1 and C_2) also suggests an alternative approach – to connect the gate to the drain of the other branch, resulting in the self-biased Colpitts configuration (Figure 29.3.2b). This topology has an effective transconductance of $-(2C_1C_2+C_2^2)g_m/(C_1+C_2)^2$, which is $(2+C_2/C_1)$ times higher than that of the standard Colpitts VCO. Furthermore, because the gate and source terminals are driven with anti-phase signals, faster commutation with better noise suppression from the differential pair is achieved.

In a standard cross-coupled VCO, the second harmonic present at the common-source node is modulated by the flicker noise from the differential pair and down-converted to the fundamental frequency, thus increasing the close-in phase noise [4]. This phenomenon does not arise in the proposed differential Colpitts topologies because there is no common-source node present, which leads to a superior close-in phase noise performance.

Finally, applying series coupling [4] to the VCO of Fig. 29.3.2b leads to the Colpitts QVCO of Fig. 29.3.2c. Optimization of the QVCO involves sizing both the switching and coupling transistors to achieve efficient current switching with minimal phase noise. On-chip transformers are used to avoid long interconnect lines and to obtain higher Q (≈10) than with the inductors (Q≈8) used in the VCO. Active tail current sources are used rather than resistors in the VCO/QVCO for better robustness at the expense of higher flicker noise.

A prototype chip is fabricated in a standard 6-metal 0.18μm CMOS RF process. For the g_m-boosted CGLNA, a transformer turns ratio of 1:1 is chosen for demonstration purposes. Further reduction in NF is possible with A>1 using a larger turns ratio. The measured S-parameters (Fig. 29.3.3) show S_{21} of 9.4dB peaking at 5.8GHz. The LNA draws only 1.9mA from 1.8V owing to the g_m-boosting technique. Measured IIP3 is 7.6dBm and NF at maximum gain is 2.5dB (Fig. 29.3.4). The proposed LNA has an excellent FOM compared to competing designs (Fig. 29.3.6). It is noted that some common-source designs achieve better noise performance at higher power consumption and with off-chip components.

The Colpitts differential VCO (Fig. 29.3.2b) operates at a center frequency of 1.79GHz with a tuning range of 22% while the Colpitts QVCO (Fig. 29.3.2c) operates from 1.83GHz to 2.24GHz for a 20% tuning range. Figure 29.3.5 shows measured phase noise plots of the VCO/QVCO. The VCO has a phase noise of –97dBc/Hz at 50kHz offset and –128dBc/Hz at 1MHz offset. It draws 3.6mA from a 2.0V supply. The QVCO draws only 4.3mA from 2.0V to attain a close-in phase noise of –104dBc/Hz at 50kHz offset. Its phase noise at 1MHz offset is –127dBc/Hz. Figure 29.3.6 compares its FOM to existing designs. The chip micrograph is shown in Fig. 29.3.7.

Acknowledgements:
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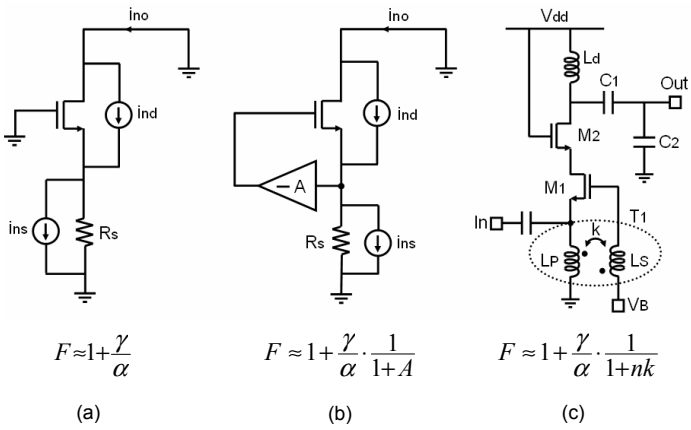

Figure 29.3.1: (a) Conventional CGLNA; g_m-boosted CGLNA with (b) active, and (c) transformer coupling.

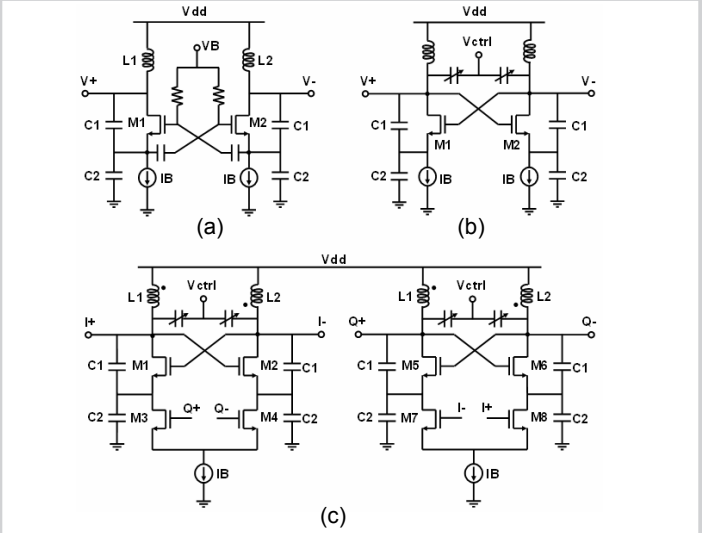

Figure 29.3.2: Evolution of g_m-boosted Colpitts oscillators. (a) Capacitor-coupled VCO with separate gate bias, (b) self-biased VCO, and (c) self-biased QVCO.

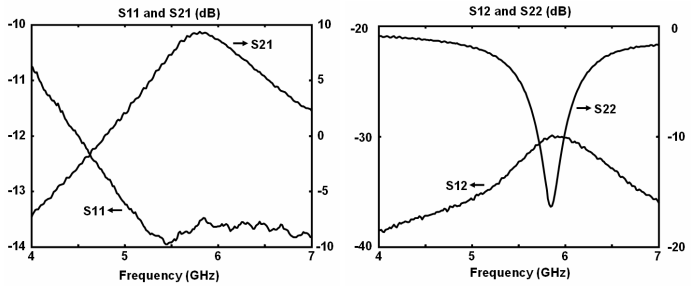

Figure 29.3.3: Measured LNA S-parameters.

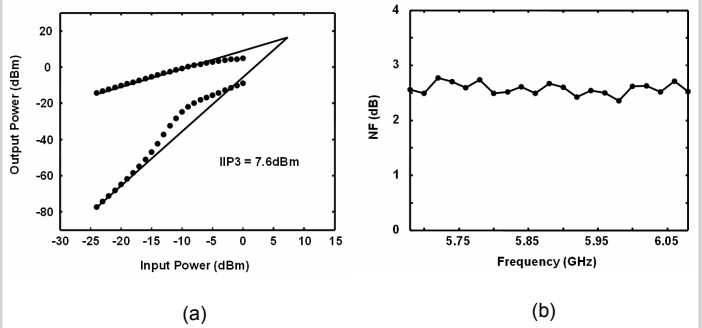

Figure 29.3.4: Measured LNA (a) IIP3, and (b) Noise Figure.

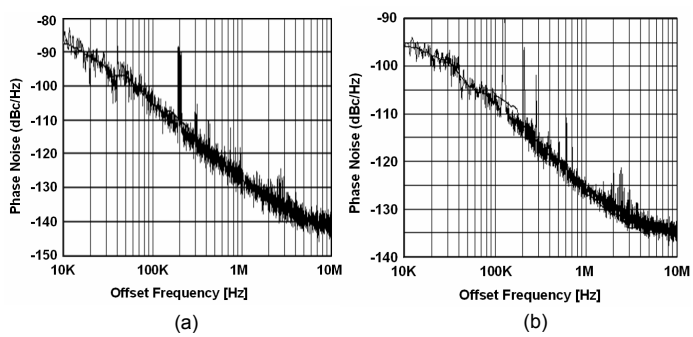

Figure 29.3.5: Measured phase noise of (a) VCO, and (b) QVCO.

Ref. LNA	CMOS Tech. (nm)	Freq. (GHz)	Power (mW)	NF (dB)	S21 (dB)	IIP3 (dBm)	Fully on-chip	$FOM = \frac{Gain_{abs}\cdot IIP3_{mW}\cdot f_{GHz}}{(F-1)\cdot P_{mW}}$
This work	180	5.8	3.4	2.5	9.4	7.6	Yes	37.0
Fujimoto JSSC02	250	7	13.8	3.3	6.2	8.4	Yes	6.3
Steyaert ISSCC02	250	1.57	8	1.5	15.5	-6.0	Yes	0.7
Youn ISSCC03	250	2.2	2X11.8	3	14.9	16.1	Yes	21.3 (differential)
Cha JSSC03	350	5.2	26.4	2.45	19.3	-6.1	No	0.6
Cassan JSSC03	180	5.75	2X8	0.9	14.2	0.9	No	9.85 (differential)

Ref. QVCO	CMOS Tech. (nm)	Freq. (GHz)	Power (mW)	Tuning Range	Tank Q	Phase Noise (dBc/Hz) @50KHz	Phase Noise (dBc/Hz) @1MHz	$FOM = 10\cdot\log_{10}[(f_o/\Delta f)^2/L\{\Delta f\}\cdot P_{mW}]$ @50KHz	$FOM = 10\cdot\log_{10}[(f_o/\Delta f)^2/L\{\Delta f\}\cdot P_{mW}]$ @1MHz
This work	180	1.83	8.6	20%	10	-104	-127	185.9	182.9
Kim JSSC02	180	1.1	5.4	28%	NA	-95	-120	174.5	173.5
Steyaert JSSC02	250	1.57	30	24%	20	-108	-138	183.2	187.1
Tiebout JSSC01	250	1.8	20	17%	8	-105	-136	183.1	188.1
Andreani ISSCC02	350	1.8	50	18%	6	-98	-133	172.1	181.1
Andreani ESSCIRC02	350	2	20.8	17%	6	-98	-130	176.9	182.8

Figure 29.3.6: LNA and QVCO performance comparisons.

Continued on Page 615

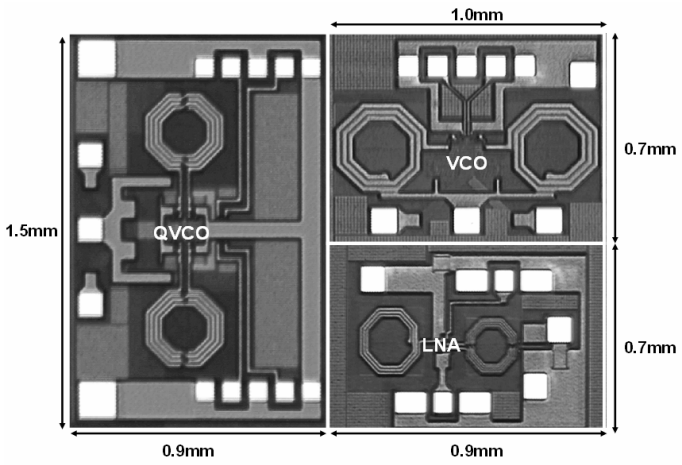

Figure 29.3.7: Chip microphotograph in 180nm CMOS.

 0-7803-8904-2/05/$20.00