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A g_m-Boosted Current-Reuse LNA in 0.18μm CMOS

Jeffrey S. Walling, Sudip Shekhar and David J. Allstot[1]

Dept. of Electrical Engineering, Univ. of Washington, Seattle, WA, 98195, USA

***Abstract*—Demand for fully-integrated RF circuits offering low power consumption continues to grow, along with a strong desire for high performance. In this paper a design that enhances the performance of the common-gate LNA is detailed. The noise performance is improved through the use of a g_m-boosting technique, while the gain performance is improved using current-reuse techniques. The proposed solution alleviates the issues related to the common-source-common-source current-reuse topologies. The technique is validated with a design in 0.18μm CMOS, with a 5.4GHz LNA which achieves >20dB of gain, <3dB NF and consumes only 2.7mW of power.**

***Index Terms*—Current-reuse, gm-boosting, low noise amplifier, noise figure, transformer.**

I. Introduction

Portable applications such as cell phones, WLAN transceivers and sensor networks strive to meet stringent performance requirements with the lowest power consumption, in order to preserve battery life. In a receiver front-end, a low noise amplifier needs to attain a large gain and low noise with the minimum possible power consumption and area. An attractive solution is a g_m-boosted common-gate (CG) LNA [1][2]. Compared to its fully-integrated common-source (CS) counterpart, it uses much less current and area (number of inductors) to achieve comparable noise performance. However, the finite quality factor of on-chip inductors in CMOS has limited the gain of a CG-LNA to about 10-12dB, which may not be sufficient in some applications.

To realize high gain (>15dB) and low power, a CS-CS cascaded LNA has been proposed [3][4], where the second stage shares (i.e., reuses) the bias current of the first-stage to save power. In Fig. 1(a), a CS second stage is cascaded upon a CS first stage to reuse the bias-current. The output of the first stage is connected to the input of the second through a large coupling-capacitor (C_c); another large bypass-capacitor (C_b) is used at the source of M_2 to provide an ac ground. Although more power efficient and stable than a single-stage CS-LNA with comparable (high) gain, it still suffers from several drawbacks: (a) Frequency alignment of the resonant frequencies of the three high-Q tanks is difficult owing to process, voltage, and temperature (PVT) variations. (b) The reverse isolation of a CS stage is inherently poor. When the gain is high, the resultant larger feedback to the input raises stability concerns [4]. (c) The small parasitic substrate impedance seen at node X of M_1 degrades the quality factor of the tank connected at this node. The LNA design of Fig. 1(b) solves the latter two problems [4]; however, as it uses four on-chip and two off-chip inductors, it is not fully integrated and occupies more chip area. The approach is even more cumbersome in differential implementations.

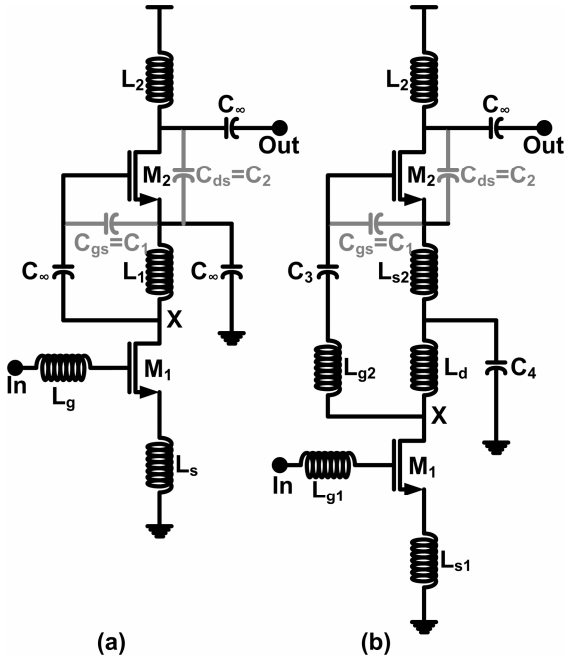

Fig. 1. Previously proposed current-reuse LNAs [3][4].

A g_m-boosted current-reuse CG-CS LNA is introduced in this paper. It achieves noise and gain performance comparable to a CS-CS current-reuse LNA, and consumes considerably less power and chip area. It mitigates the noise, gain, robustness, stability, and integration issues associated with previous solutions. Section II presents the theory of operation for the proposed LNA. Section III gives the measured results, and Section IV concludes the paper.

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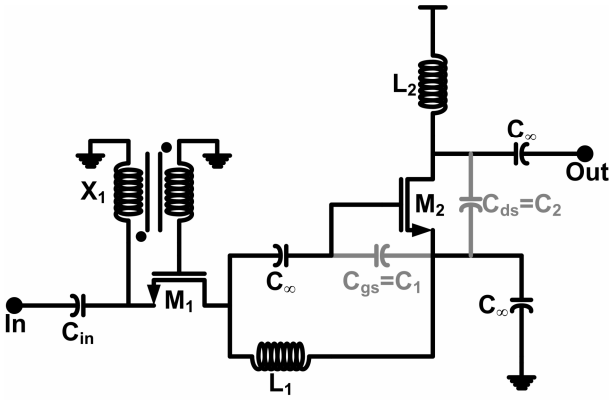

Fig. 2. A transformer g_m-boosted current-reuse LNA. Bias details are not shown.

II. Theory of Operation

A schematic of the proposed LNA is shown in Fig. 2. The CG-LNA has better reverse isolation and robustness than a CS-LNA [1]. Thus, the use of a CG input stage improves stability over the design of Fig. 1(a). Furthermore, the CG input stages uses just one on-chip spiral inductor, which improves its ability to be integrated compared to the designs of Fig. 1. Analysis of the LNA starts with a determination of its gain followed by a derivation of its noise performance.

A. Gain Analysis

A simple small-signal model of the CG stage is shown in Fig. 3. The transformer, X_1, has been replaced by an ideal stage with gain $-A$. This assumption is valid provided the winding inductance connected to the source of M_1 resonates with the total capacitance seen looking into the source. It is shown in [1] that $A=nk$, where n is the turns ratio, k is the coupling factor of the transformer, and C_1 represents the capacitance seen looking into the gate of the CS stage. C_1 along with L_1 and the output resistance of M_1 form a parallel resonant network with a voltage gain given by:

$$A_{v,CG} = \left[g_m\left(1+A\right)r_{o1}+1\right]\frac{s/r_{o1}C_1}{s^2+s/r_{o1}C_1+1/L_1C_1} \quad (1)$$

Substituting $k_1=g_{m1}(1+A)r_{o1}+1$, $\omega_{01}^2=1/(L_1C_1)$, and $\omega_{01}/Q_1=1/(r_{o1}C_1)$ yields:

$$A_{V,CG} = k_1\frac{s\left(\omega_{01}/Q_1\right)}{s^2+s\left(\omega_{01}/Q_1\right)+\omega_{01}^2} \quad (2)$$

The combination of r_o, L_1, and C_1 forms a parallel resonant circuit with gain k at the center frequency w_0.

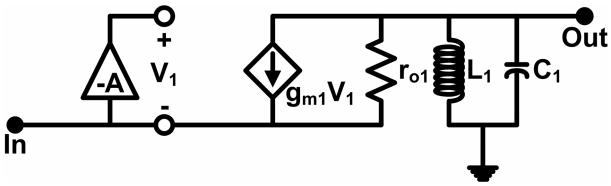

Fig. 3. Small-signal model of a g_m-boosted CG LNA stage.

A simple small-signal equivalent circuit of the CS stage is displayed in Fig. 4. C_2 is the total capacitance seen at the drain of M_2 in parallel with any load capacitance. The combination of L_2 and C_2 and the output resistance of M_2 (r_{o2}) form a parallel resonant network with the voltage gain given by:

$$A_{v,CS} = -g_{m2}r_{o2}\frac{s\left(1/C_2\right)}{s^2+s\left(1/r_{o2}C_2\right)+1/L_2C_2} \quad (3)$$

Substituting $k_2=g_{m2}r_{o2}$, $\omega_{02}^2=1/(L_2C_2)$, and $\omega_{02}/Q_2=1/(r_{o2}C_2)$ yields:

$$A_{v,CS} = -k_2\frac{s\left(\omega_{02}/Q_2\right)}{s^2+s\left(\omega_{02}/Q_2\right)+\omega_{02}^2} \quad (4)$$

Hence, the total gain of the cascaded amplifier is:

$$A_{v,T} = -k_1k_2\frac{s\frac{\omega_{02}}{Q_2}}{s^2+s\frac{\omega_{02}}{Q_2}+\omega_{02}^2}\frac{s\frac{\omega_{01}}{Q_1}}{s^2+s\frac{\omega_{01}}{Q_1}+\omega_{01}^2} \quad (5)$$

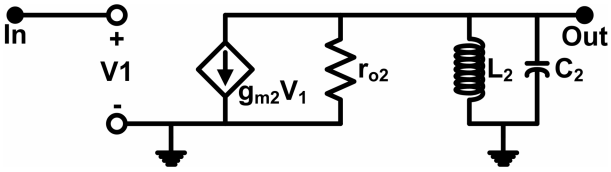

Fig. 4. Small-signal model of the CS LNA stage.

The frequency responses of a CG-CS LNA designed for ~20dB of gain at 5.4GHz are shown in Fig. 5(a). A concern expressed earlier regarding a current-reuse cascaded LNA is the difficulty of frequency aligning the three resonances. In a CG stage, the input tank is a low-Q parallel resonant tank with a fairly broadband input match. In contrast, a CS stage has a high-Q series resonance input network. Thus, the alignment difficulty is considerably reduced to matching the resonant frequencies of two tanks—formed by $L_1\|C_1$ and $L_2\|C_2$—as in a standard single-stage LNA. Due to the relatively low quality factors of the resonant networks in CMOS, the LNA gain exhibits excellent robustness to PVT variations. For example, if the load inductance and capacitance of the CG stage are each increased by 5%, while the load inductance and capacitance of the CS

stage are each decreased by 5% in (5), the overall gain decreases by only 1dB as shown in Fig. 5(b).

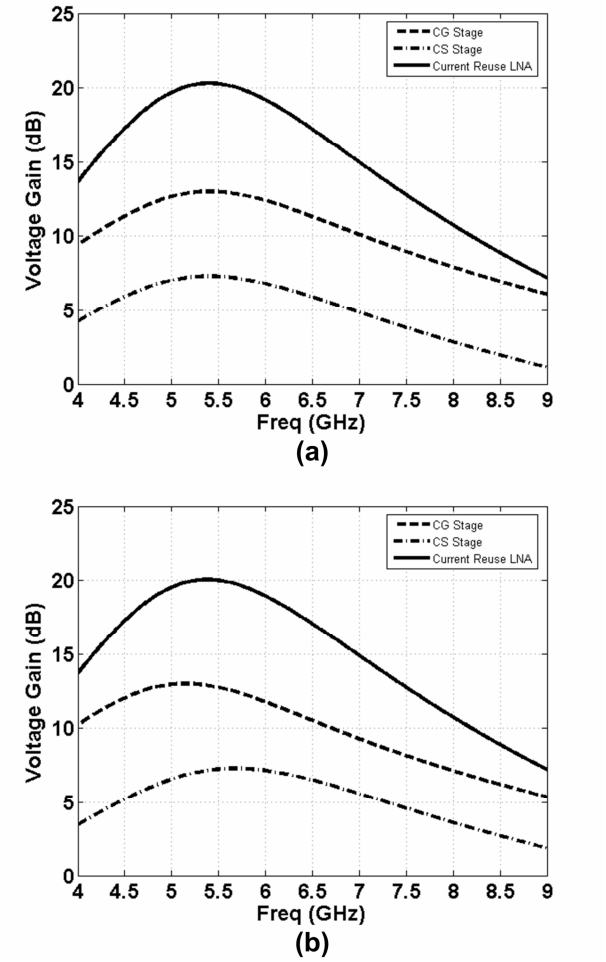

Fig. 5. Typical current-reuse LNA frequency responses derived from (5) with (a) identical resonant frequencies, and (b) 5% component mismatches.

B. Noise Analysis

A simple small-signal noise model for the g_m-boosted CG stage (Fig. 6) includes the dominant noise sources, i_{nD} and i_{nRs}, along with the induced gate noise, i_g [1]. In conventional common-gate configurations, the induced gate noise is usually insignificant; however, it becomes significant in the g_m-boosted configuration as the turns ratio, $n = (L_P/L_S)^{1/2}$, is increased. The noise factor of the CG-stage is [1]:

$$F = 1 + \frac{\gamma}{\alpha}\frac{m}{1+nk} + \frac{\delta\alpha}{5m}\left(\frac{\omega}{\omega_T}\right)^2 \frac{\left(1+2nk+n^2\right)^2}{\left(1+nk\right)^3} \qquad (6)$$

where $m = 1/(g_m R_S)$, and γ and δ are empirical parameters associated with a specific device. As noted in [1], there is an optimum turns ratio, n, for a given coupling factor, k. However, the transformer design required to realize this non-integer coupling factor is considerably complicated. If a typical value of $k = 0.7$ is used with a 1:1 transformer ($n = 1$), the noise factor is:

$$F = 1 + \frac{\gamma m}{1.7\alpha} + \frac{\delta\alpha}{2}\left(\frac{\omega}{\omega_T}\right)^2 \qquad (7)$$

With typical numbers substituted in (6) for a 0.18µm CMOS process ($\gamma = 2$, $\delta = 4$, $\alpha = 0.85$ and $m = 0.7$) and the transistor operating at one-tenth its transition frequency, the noise figure is approximately 3.0dB.

Similarly, for the CS-stage, the noise factor is

$$F = 1 + \frac{\gamma m}{\alpha} + \frac{\delta\alpha}{5m}\left(\frac{\omega}{\omega_T}\right)^2 \qquad (8)$$

where $m = 1/(g_m R_{out1})$. Using the same values of process parameters, the noise figure is about 4.2 dB.

When cascading two LNA stages, the gain of the first stage reduces the contributions of the latter stage to the overall noise factor according to the Friis equation:

$$F_T = F_1 + \left(F_2 - 1\right)/G_1 \qquad (9)$$

Using the noise figures calculated above ($NF_1 = 3.1$dB and $NF_2 = 4.2$dB), and the gain distribution shown in Fig. 5 ($G_1 = 13.5$dB and $G_2 = 7.5$dB), the overall noise figure of the cascaded CG-CS LNA is 3.7dB.

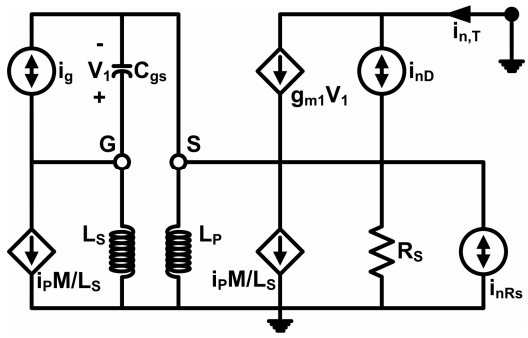

Fig. 6. Small-signal noise model for the CG stage [1].

III. MEASUREMENT RESULTS

A g_m-boosted, current-reuse LNA is fabricated in a 0.18µm CMOS process with six AlCu metal layers. A chip microphotograph of the LNA is shown in Fig. 7. It consumes 1.5mA of current from a 1.8V supply at the maximum gain setting. The gain is varied from 14-21dB by changing the bias voltages of the two stages. The quality of the input match depends on the bias current; hence, the gate voltage of the input CG stage is set to maintain a reasonable S_{11} (< -10dB). The gate voltage of the output CS stage is set high enough to keep the CG stage in saturation.

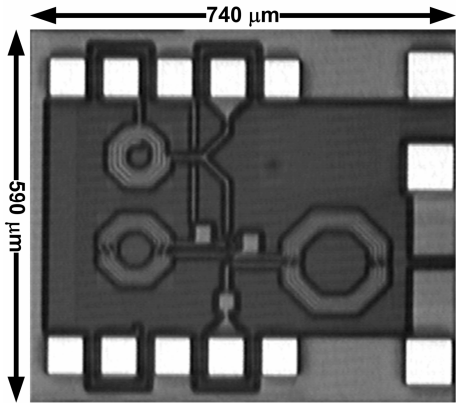

Fig. 7. Photograph of the g_m-boosted, current-reuse LNA.

The S-parameters of the LNA as measured using an *Agilent E8364 Performance Network Analyzer* are displayed in Fig. 8.

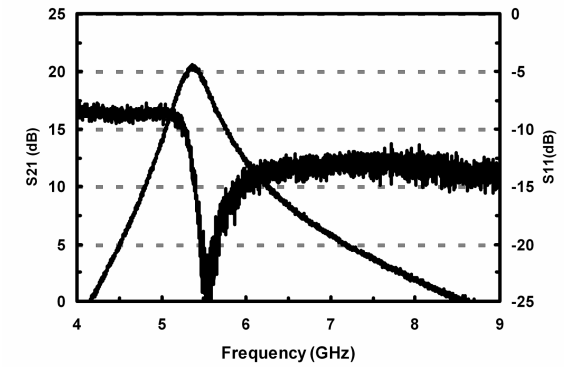

Fig. 8. LNA S-parameters for the maximum gain setting.

The noise figure of the LNA is measured using an Agilent N8975A Noise Figure Analyzer; the measured value for the maximum gain mode is shown in Fig. 9.

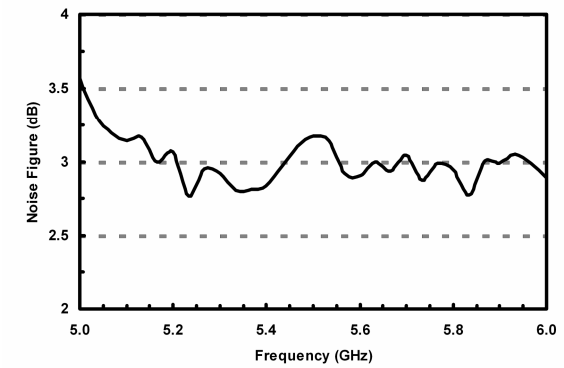

Fig. 9. NF measured for the LNA in its maximum gain setting.

The measured gains for four different bias conditions are shown in Fig. 10. When biased for maximum and minimum gains, the LNA draws 1.5mA and 0.8mA, respectively, from a single 1.8V power supply. The input match is maintained for the full-range of gain settings with S_{11} < -10dB across the frequency band of operation. Finally, it should be noted that one of the drawbacks associated with this technique is degraded linearity performance, due to large gain from the first stage being input into a second stage with similar bias conditions (low dc current). The measured OIP_3 of this amplifier in the high gain mode is -2 dBm. Thus, there is a tradeoff between linearity and power consumption in a current-reuse LNA.

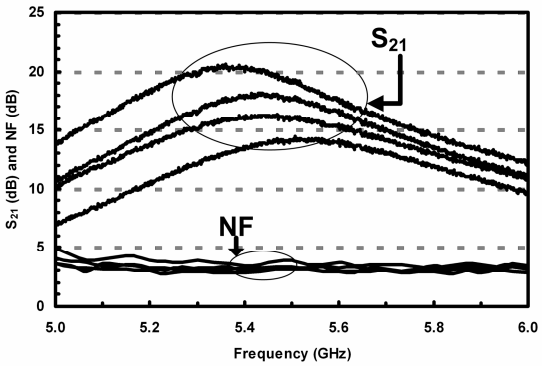

Fig. 10. LNA gains and noise figures measured for four different bias settings. Case 1 (topmost curve) is maximum gain, and case 4 (lowest gain curve) is minimum gain.

IV. Conclusions

A g_m-boosted current-reuse CG-CS LNA is presented that demonstrates NF and gain performance comparable to most CS-CS current-reuse LNAs, and operates with less power and chip area.

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