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CMOS VCO and LNA Using Tuned-Input Tuned-Output Circuits

Sudip Shekhar, *Student Member, IEEE*, Jeffery S. Walling, *Student Member, IEEE*, Sankaran Aniruddhan, *Member, IEEE*, and David J. Allstot, *Fellow, IEEE*

***Abstract*—A tuned-input tuned-output (TITO) VCO utilizes two resonant-tanks to achieve a low measured phase noise of −130.5 dBc/Hz @ 1 MHz offset from 2.5 GHz center frequency. Improvement in phase noise is achieved with comparable power consumption and tuning range compared to a cross-coupled VCO topology. A TITO cell similar to that in the VCO is used as a common-source amplifier in a current-reuse configuration cascaded with a g_m-boosted common-gate amplifier to realize a high gain (>20 dB), low power (2.7 mW) LNA. A technique to improve the linearity of the current-reuse LNA is also presented.**

***Index Terms*—Current reuse, linearity, low-noise amplifier, noise figure, phase noise, tuned-input tuned-output, TITO, voltage-controlled oscillator.**

I. Introduction

THE voltage-controlled oscillator (VCO) and low-noise amplifier (LNA), which are critical blocks in a CMOS RF receiver, have attracted tremendous attention in the past decade. Stringent adjacent channel suppression requirements have driven VCO research towards the goal of extremely low phase noise. Of course, the phase noise specification must be met within a limited power budget, and using a nanometer CMOS technology for its cost and scale-of-integration advantages. A conventional CMOS cross-coupled VCO is a good choice in terms of power dissipation, reliable start-up and tuning range. However, its phase noise performance is not adequate for demanding applications. For a low-noise amplifier (LNA), which constitutes the first stage of a CMOS RF receiver, high gain and low noise figure must also be achieved with minimum power dissipation. The power consumption constraint is especially severe in low-power portable receivers and sensor-network applications. An inductively degenerated common-source LNA (CSLNA) is attractive in terms of gain and noise figure, but expensive in terms of power consumption. A g_m-boosted common-gate LNA (CGLNA) draws less current than its common-source counterpart, but offers only moderate gain; e.g., ∼10 dB in a 0.18 μm CMOS process with on-chip inductor Q ∼10 [1]. Obviously, this is not sufficient for applications where high gain (> 15 dB) is needed. Thus, there is a need for an LNA architecture that realizes the high gain of CSLNA with the low power of CGLNA.

An oscillator and amplifier share an important characteristic: an amplifier can be configured to oscillate through positive feedback. Fig. 1 shows a common-source amplifier cell with two resonant circuits—inductors L_d and L_g and capacitors C_d and C_g comprise the drain and gate tanks, respectively, and C_f is the gate-drain capacitor. With proper biasing and sizing so that C_f is small, this cell acts as an amplifier. On the other hand, if C_f is designed to be larger, the same cell constitutes an oscillator because the resultant positive feedback satisfies the necessary conditions for oscillation. A tuned-input tuned-output (TITO) oscillator that uses the amplifier cell in the positive feedback regime is presented in Section II. The theory of operation is presented, and expressions are derived for the frequency of oscillation, reliable start-up, and phase noise power spectral density. Section III introduces the design and implementation of a TITO CMOS differential VCO [2]. In Section IV, the amplifier cell of Fig. 1 is used as a current-reuse cascade stage in a g_m-boosted common-gate LNA [3]. The gain, noise figure, and linearity of the so-called current-reuse LNA (IRLNA) are derived in Section V. An improved version of IRLNA is proposed in Section VI with enhanced linearity, the so-called EL-IRLNA. Measurement results for the TITO-based VCO and LNA prototypes are presented in Section VII, and conclusions are drawn in Section VIII. Derivations for the general start-up and frequency of oscillation characteristics for the VCO are presented in Appendix A, and equations for IIP3 for a common-source LNA are given in Appendix B.

II. TITO Theory of Operation

The amplifier cell of Fig. 1 forms the basis of the tuned-input tuned-output CMOS oscillator, which is adapted from its classical tuned-grid tuned-plate counterpart [4]. The drain tank is designed to behave inductively at the frequency of oscillation. Consequently, the inductive load in conjunction with the action of the feedback capacitor, C_f, forms the negative impedance needed by the gate tank to initiate oscillation [5]. Next, the frequency of oscillation and start-up condition for the TITO oscillator are determined for the special case of identical tanks; i.e., $L_d = L_g = L$, and $C_d = C_g = C_v$; the general case is treated in Appendix A. In Fig. 1, assume C_g (C_d) includes C_{gs} (C_{ds}) of M_1 and other parasitic capacitances at the gate (drain) node, and

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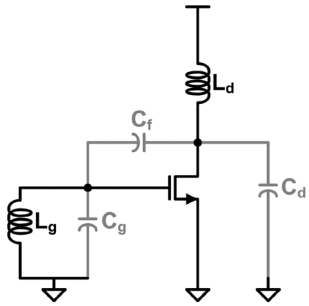

Fig. 1. Common-source nMOS tuned-input tuned-output (TITO) amplifier cell.

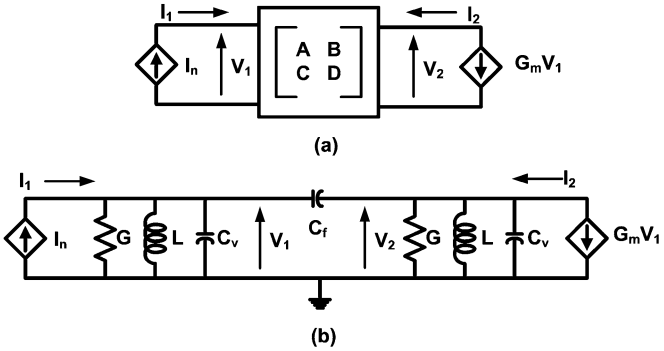

Fig. 2. (a) General representation of a feedback oscillator with the passive circuit represented as an ABCD matrix [6]. (b) Equivalent circuit for the TITO oscillator.

C_f includes C_{gd} of M_1. The oscillation frequency, start-up condition, and phase noise spectral density of the oscillator are derived using the techniques of Nallatamby *et al.* [6]. Consider an ABCD representation of a feedback oscillator [Fig. 2(a)] and an equivalent circuit of the TITO oscillator [Fig. 2(b)]. The white noise source, I_n, is the transistor noise, G_m is the transconductance of the transistor, and G is the equivalent conductance of both tanks. It is assumed that the Q-factor of the tank is limited by inductor losses only.

The ABCD coefficients are determined using nodal analysis

$$A = A_R + jA_I = \left(1 + \frac{C_v}{C_f} - \frac{1}{\omega^2 L C_f}\right) - j\frac{G}{\omega C_f} \tag{1}$$

$$B = jB_I = -j\frac{1}{\omega C_f} \tag{2}$$

$$C = C_R + jC_I = 2G\left(1 + \frac{C_v}{C_f} - \frac{1}{\omega^2 L C_f}\right) + j\left(\omega(2C_f + C_v)\frac{C_v}{C_f} - \frac{1}{\omega}\left(\frac{2}{L}\left(1 + \frac{C_v}{C_f}\right) + \frac{G^2}{C_f}\right) + \frac{1}{\omega^3}\frac{1}{L^2 C_f}\right) \tag{3}$$

$$D = A. \tag{4}$$

A. Frequency of Oscillation

The frequency of oscillation, ω_0, is obtained by setting $C_I(\omega_0) = 0$ in (3) [6]

$$\omega_0 = \frac{1}{\sqrt{1 + (G^2 L/2C_f)}}\frac{1}{\sqrt{L(C_v + 2C_f)}}. \tag{5}$$

For a parallel-resonant circuit, $G = 1/\omega QL$. It can be shown that $G^2 L/2C_f \ll 1$, and hence

$$\omega_0 = \frac{1}{\sqrt{L(C_v + 2C_f)}}. \tag{6}$$

The frequency of oscillation in the case of unequal tank components and neglecting the tank conductance is (Appendix A)

$$\omega_0 = \sqrt{\frac{\frac{C_g + C_f}{L_d} + \frac{C_d + C_f}{L_g} - \sqrt{\frac{4C_f^2}{L_d L_g} + \left(\frac{C_g + C_f}{L_d} - \frac{C_d + C_f}{L_g}\right)^2}}{2(C_d C_f + C_f C_g + C_g C_d)}}. \tag{7}$$

B. Start-Up Condition

The start-up condition is given by $-G_m = C_R(\omega_0)$ [6]; hence, from (3) and (6)

$$-G_{m,\min} = -2G. \tag{8}$$

Thus, for reliable start-up, the small-signal transconductance of the active device should exceed twice the conductance of the tank at the frequency of oscillation.

For dissimilar tanks, the start-up condition is (Appendix A)

$$-g_m = G_d\left(1 + \frac{C_g}{C_f} - \frac{1}{\omega^2 L_g C_f}\right) + G_g\left(1 + \frac{C_d}{C_f} - \frac{1}{\omega^2 L_g C_f}\right). \tag{9}$$

C. Phase Noise

Leeson's model [7] predicts the phase noise of a *single*-resonator feedback network as

$$S_{\Delta\phi\text{out}} = S_{\Delta\phi\text{in}}\left[1 + \left(\frac{\omega_0}{2Q_{\text{load}}\Delta\omega}\right)^2\right] \tag{10}$$

where $S_{\Delta\phi\text{out}}$ and $S_{\Delta\phi\text{in}}$ are the phase noise power spectral densities of the output and input, respectively, at a frequency offset, $\Delta\omega$, from the oscillation frequency, ω_0, and Q_{Load} is the *oscillator loaded* Q, which is, in general, different from the Q of the passive tank circuit. Equation (10) is valid for *all* oscillators if Q_{Load} is defined as [6]

$$Q_{\text{load}}(\omega_0) = \frac{\omega_0}{2}\left|\frac{d\phi}{d\omega}\right|_{\omega_0} = \frac{\omega_0}{2}\left|\frac{1}{C_I}\frac{dC_I}{d\omega}\right|_{\omega_0}. \tag{11}$$

For the TITO oscillator, (3) and (6) lead to

$$C_I|_{\omega_0} = -2G \tag{12}$$

$$\left|\frac{dC_I}{d\omega}\right|_{\omega_0} = -4(2C_f + C_v)\left(1 - \frac{G^2 L}{4C_f}\right) \approx -4(2C_f + C_v). \tag{13}$$

Substituting (12) and (13) into (11) with $G = 1/\omega QL$ gives

$$Q_{\text{load}}(\omega_0) = \frac{\omega_0}{2}\frac{2(2C_f + C_v)}{G} = Q\omega_0^2 L(2C_f + C_v) = Q. \tag{14}$$

Thus, the *loaded* Q of the TITO oscillator is identical to the Q of the passive tank. Although the TITO VCO employs two

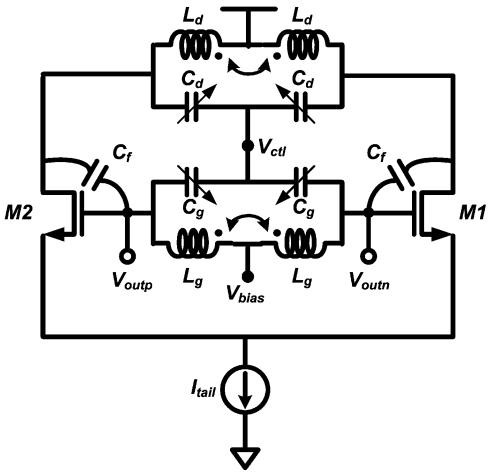

Fig. 3. A fully differential CMOS TITO VCO.

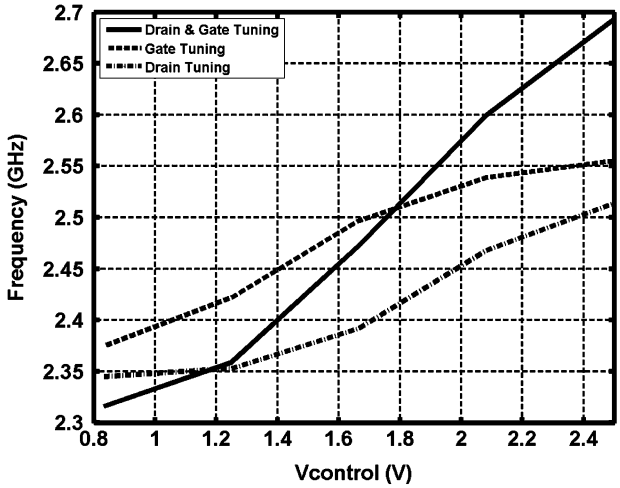

Fig. 4. Simulated tuning range plots for the TITO VCO. Tuning range is increased when both tanks are tuned together rather than just gate- or drain-tuning alone.

resonant tanks, its phase noise dependence on Q at an offset frequency $\Delta\omega$ is similar to that of other *LC* oscillators.

D. Tank Characteristics at ω_0

At the frequency of oscillation, the admittance of the drain tank is

$$\mathbf{Y}_{\mathrm{d}}(\omega_0) = G - \frac{j}{\omega_0 L\left(1+\frac{C_v}{2C_f}\right)} = G - j2\omega_0 C_f. \qquad (15)$$

Hence, as claimed earlier, the drain tank acts *inductively* at ω_0, and its inductance is enhanced by $(1 + C_v/2C_f)$. Clearly, it is operating below its self-resonant frequency:

$$\omega_{\mathrm{self}} = \frac{1}{\sqrt{LC_v}} < \frac{1}{\sqrt{L(C_v+2C_f)}} = \omega_0. \qquad (16)$$

The *stand-alone* gate tank shows the same behavior. However, its enhanced inductance resonates with the effective feedback capacitance $(2C_f)$ at the oscillation frequency ω_0 (6).

III. Fully Differential TITO VCO

A. Implementation and Design Tradeoffs

Two identical branches (Fig. 1) are connected at their source nodes, and biased through an nMOS tail current source to achieve a differential configuration (Fig. 3). The bias tail current is set for optimum thermal and flicker-noise performance and adequate output voltage headroom. L_g and L_d are implemented as center-tapped symmetrical inductors, which saves die area, simplifies layout, and increases the Q of the tanks.

The gate and drain tank capacitors are realized using identical varactors (C_v). Fig. 4 plots the tuning range of the VCO as the varactor control voltage is varied for three cases: 1) fixed gate varactors and tuned drain varactors (6.95% tuning range); 2) fixed drain varactors and tuned gate varactors (7.35% tuning range); and 3) both gate and drain varactors tuned together (15.05% tuning range). Clearly, the overall tuning range is highest when the drain tank is tuned along with the gate tank over a range of frequencies.

The choice of C_f is determined by a trade-off between the overall tuning range and reliable start-up. A smaller C_f provides a wider tuning range (6), but a larger C_f ensures an easier start-up (9). As a practical matter, C_f should be much larger than the intrinsic gate-drain overlap capacitance (C_{gd}) of the nMOS switching devices to ensure that the VCO characteristics are independent of parasitic capacitance, which is critical for robust operation with respect to process, voltage, and temperature (PVT) variations. Herein, extrinsic MIM capacitances of 1 pF are added, which results in overall feedback capacitances of $C_f = C_{gd} + 1$ pF.

Another design tradeoff exists among the power consumption of the VCO, its start-up factor, and its output signal swing. The switching transistors are sized for a start-up factor ≈ 3; this choice ensures reliable functionality with respect to PVT variations but costs more DC bias current. The sizes of the active devices together with the magnitude of the DC tail current determine the output signal swing and drain current noise. Care is taken to avoid excessive signal swing, which leads to distorted sinusoidal output voltage waveforms.

B. Phase Noise

Fig. 5 shows the simulated phase noise performance of the TITO VCO at $f_0 = 2.5$ GHz along with that of a complementary cross-coupled VCO (CCC-VCO) with identical power consumption, tuning range, and tank Q. The TITO VCO is superior by 6.4 dBc at 100 kHz offset, and 5.6 dBc at 1 MHz offset because of its better impulse-sensitivity characteristic [5]. Fig. 6 shows the simulated drain voltage and current of M_1. Clearly, most of the drain current flows only during the minimum of the tank voltage, and as a consequence, most of the drain noise is injected when the tanks are insensitive to noise perturbations. From this viewpoint, a TITO VCO resembles a Hartley or Colpitts oscillator.

Fig. 7 shows the simulated phase noise of the TITO VCO across its tuning range. Phase noise curves are also shown when

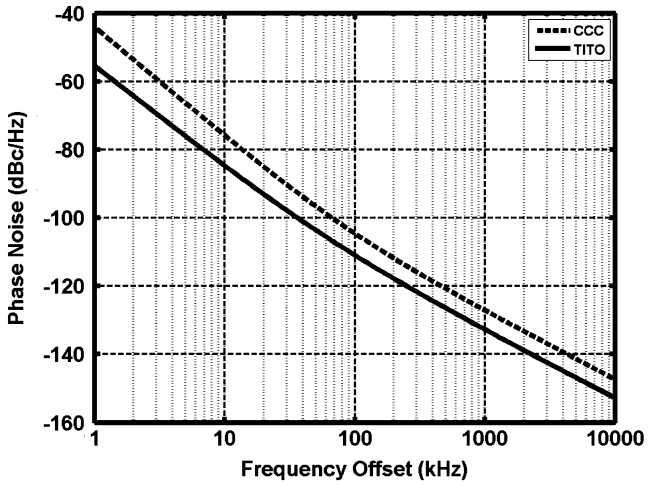

Fig. 5. Simulated phase noise power spectral density of the TITO VCO compared to a CCC-VCO.

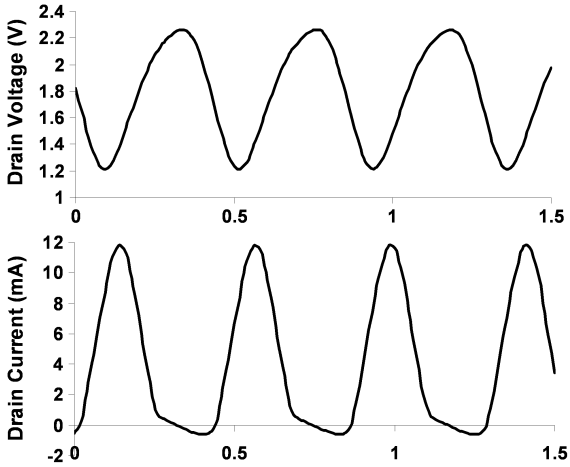

Fig. 6. Simulated transient waveforms for the drain current and voltage at the drain node of M_1.

only one of the tanks is tuned. The corresponding characteristic for a CCC-VCO is also shown.

IV. Current Reuse LNA

A. Previous Work

Designing a high-gain (>15 dB) LNA in a single-stage is challenging in fine-line CMOS because of the finite Q of on-chip inductors. It is relatively easy to realize moderate gain (10–15 dB) in a CSLNA (compared to a CGLNA) at the cost of increased power consumption and decreased stability. However, the current-reuse LNA (IRLNA) offers a means to obtain higher gain (>15 dB) without these undesirable trade-offs [8], [9]. An IRLNA usually comprises a cascade of two amplifiers separated by a network that strategically redirects the AC and DC currents. The DC current flows through both stages (*current-reuse*) and the AC signal is amplified by both. Previous implementations of IRLNA use a CS-CS cascade [8], [9]; consequently, the limitations associated with a CS input

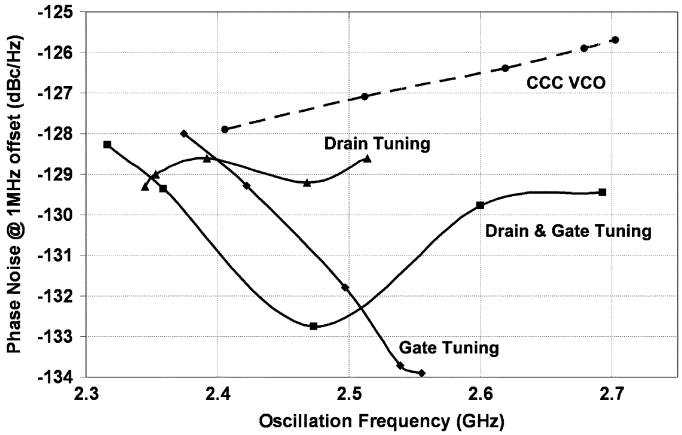

Fig. 7. Simulated phase noise power spectral density at a 1 MHz offset frequency across the tuning range of the TITO VCO and CCC-VCO.

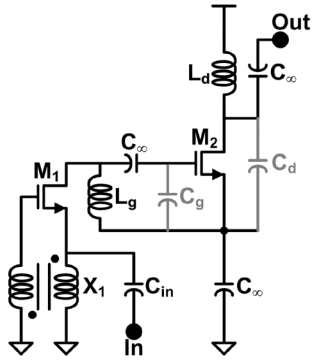

Fig. 8. A g_m-boosted common-gate common-source current reuse LNA (IRLNA).

stage are incurred. Specifically, a high-Q input matching network is needed to achieve good noise performance, which, in turn, mandates either off-chip or large-area on-chip inductors. Moreover, a high-Q input matching network is necessarily narrowband and, therefore, susceptible to PVT variations, etc. Finally, it is difficult to align the resonant frequencies of the three high-Q tanks, and the modest reverse isolation of CSLNA adds to the design difficulty.

B. G_m-Boosting CG-CS IRLNA

A CGLNA exploits a simple (i.e., robust) broadband input matching network [1]. Its reverse isolation and power consumption are superior to its CSLNA counterpart, and g_m-boosting further improves its noise performance and power dissipation [1]. To achieve high gain, a g_m-boosted CGLNA is cascaded with a CSLNA in a current-reuse fashion as shown in Fig. 8. The input signal is applied at the source of M_1 and also fed out-of-phase to its gate by the transformer action of X_1, which increases its transconductance to $(1+A)g_m$ where $-A$ is the transformer gain [1]. The output of the CG stage is connected to the input of the CS stage through a large coupling capacitor, and an AC ground is realized at the source of M_2 using a large bypass capacitor. C_d at the drain tank includes C_{ds} of M_2 and the parasitic capacitance of L_d, C_g at the gate tank includes C_{gs} of M_2 and the parasitic capacitance of L_g, and C_f (not shown)

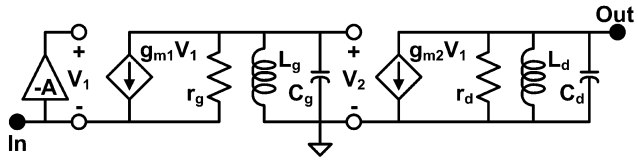

Fig. 9. Small-signal model of the IRLNA.

comprises C_{gd} of M_2. Care is taken to size M_2 so that C_{gd} is kept small. The gain, noise and linearity characteristics of the g_m-boosted IRLNA are presented in the next section.

V. Theory of Operation of Current Reuse LNA

A. Gain

A small-signal model of the current reuse amplifier is shown in Fig. 9. The transformer, X_1, of Fig. 8 is replaced by an ideal stage with a gain of $-A$, which is a valid approximation assuming its winding inductance resonates with the capacitance at the source of M_1. Using nodal analysis, the gain is

$$A_v = -g_{m2}r_d[g_{m1}(1+A)r_g+1] \times \frac{\frac{s}{r_gC_g}}{s^2+\frac{s}{r_gC_g}+\frac{1}{C_gL_g}} \frac{\frac{s}{r_dC_d}}{s^2+\frac{s}{r_dC_d}+\frac{1}{C_dL_d}}. \quad (17)$$

As expected, the overall cascade amplifier response is the product of second-order bandpass responses owing to the parallel resonant circuits at the drains of both stages. With $\omega_{0g}^2 = 1/(L_gC_g), \omega_{0d}^2 = 1/(L_dC_d), \omega_{0g}/Q_g = 1/(r_gC_g), \omega_{0d}/Q_d = 1/(r_dC_d)$, and DC gains of $k_1 = g_{m1}(1+A)r_g + 1$ and $k_2 = g_{m2}r_d$,

$$A_v = -k_1k_2 \frac{s\left(\frac{\omega_{0g}}{Q_g}\right)}{s^2+s\left(\frac{\omega_{0g}}{Q_g}\right)+\omega_{0d}^2} \frac{s\left(\frac{\omega_{0d}}{Q_d}\right)}{s^2+s\left(\frac{\omega_{0d}}{Q_d}\right)+\omega_{0d}^2}. \quad (18)$$

Here, $r_g = r_{o1}\|1/G_g, r_d = r_{o2}\|1/G_d, r_{o1}(r_{o2})$ is the output resistance of M_1 (M_2), and G_g (G_d) is the gate (drain) tank conductance. Thus, the gain response is that of a fourth-order filter. One concern for such a system is that the overall gain is degraded if the resonant frequencies of the tanks are not properly aligned. Fortunately, this concern is mitigated by the relatively low small-signal output resistance of the transistors; as a consequence, the Q is typically $\sim$3–6 so that the gain degradation is less than ~ 1 dB even for a 5% misalignment in resonant frequencies.

B. Noise

Noise analysis is accomplished by first analyzing the individual noise performances of the CG and CS stages. For an input-matched g_m-boosted CG stage, the noise factor, F, is given by [1]

$$F_{\rm CG} = 1+\frac{\gamma}{\alpha}\frac{m}{1+nk}+\frac{\delta\alpha}{5m}\left(\frac{\omega}{\omega_T}\right)^2\frac{\left(1+2nk+n^2\right)^2}{\left(1+nk\right)^3} \quad (19)$$

where α, γ, and δ are empirical device parameters and $m = 1/(g_{m1}R_s)$. It appears from (19) that optimum noise performance is achieved with the turns-ratio, n, optimized for a given coupling factor, k. As a practical matter, however, nearly optimum noise performance is attained for a transformer with $n = 1$; this design choice avoids the complexity associated with the design and layout of non-unity transformers. For an $n = 1$ transformer with coupling factor $k = 0.7$, the noise factor simplifies to

$$F_{\rm CG} \approx 1+\frac{\gamma m}{1.7\alpha}+\frac{\delta\alpha}{2}\left(\frac{\omega}{\omega_T}\right)^2. \quad (20)$$

For a CS stage without inductor degeneration, the noise factor is

$$F_{CS} \approx 1+\frac{\gamma m}{\alpha}+\frac{\delta\alpha}{5m}\left(\frac{\omega}{\omega_T}\right)^2 \quad (21)$$

where $m = 1/(g_{m2}r_d)$. The similarity of (20) and (21) is due to the absence of the Q-enhancement associated with the popular inductor-degenerated CSLNA.

The familiar Friis formula is used to calculate the total noise figure for the system [10]

$$F_{\rm CG-CS} = F_{\rm CG}+\frac{(F_{\rm CS}-1)}{A_{v,\rm CG}}. \quad (22)$$

Because the gain of the common-gate stage is relatively large, the input-referred noise contribution from the CS stage is insignificant; in other words, the absence of Q-enhancement does not significantly degrade the noise performance of the cascaded amplifier.

C. Linearity

A general limitation of current reuse topologies is that the current in the CS cascade stage is set by the input stage. If current consumption is low as desired of current reuse LNAs in the first place, linearity of the CS stage is poor. Using the direct distortion calculation method of Wambacq, *et al.* [11], a simple approximation for IIP3 of a CS stage is found (Appendix B)

$$\text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{g_m}{K_{3gm}}\right|\omega_1\omega_2C_g^2} \quad (23)$$

where g_m is the small-signal transconductance of the amplifier and K_{3gm} is the second derivative of the small-signal transconductance with respect to input voltage. The frequencies ω_1 and ω_2 represent the two tones that would be applied in a two-tone test. A small bias current gives a small g_m, which, in turn, restricts linearity. The gain of the first stage should be large to minimize the noise contribution of the second stage. Consequently, the overall linearity of the amplifier is limited by the linearity of the second CS stage.

A CG input stage is usually biased at a low DC current due to impedance matching requirements. Although desirable from a power dissipation standpoint, it implies that the CS stage will have poor linearity. Hence, the overall linearity of a CG-CS cascade is relatively poor.

VI. An Enhanced-Linearity Current Reuse LNA

Linearity of the IRLNA is modest owing to constraints on bias currents and power dissipation. Equation (23) suggests that linearity is improved with higher transconductance, which is achieved with a higher bias current in the CS transistor. To this

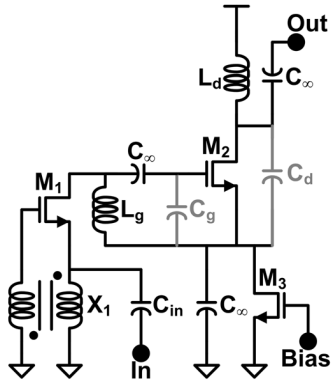

Fig. 10. Enhanced-linearity current reuse LNA (EL-IRLNA).

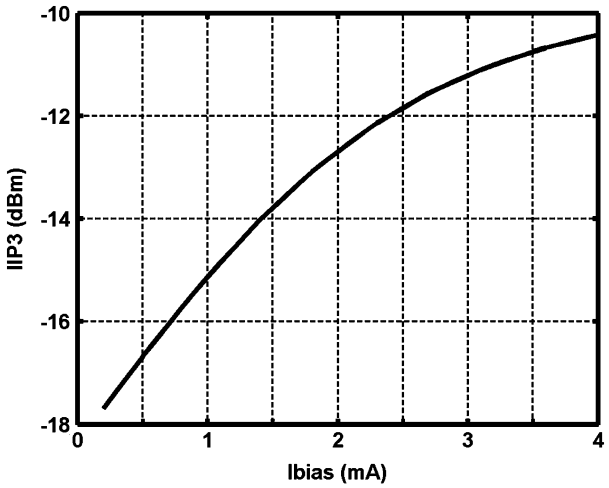

Fig. 11. Simulated IIP3 versus additional bias current for the EL-IRLNA.

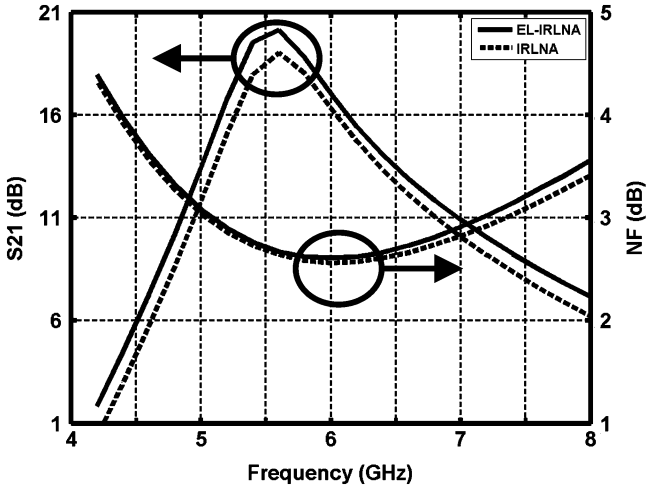

Fig. 12. Simulated gain and NF of EL-IRLNA and IRLNA.

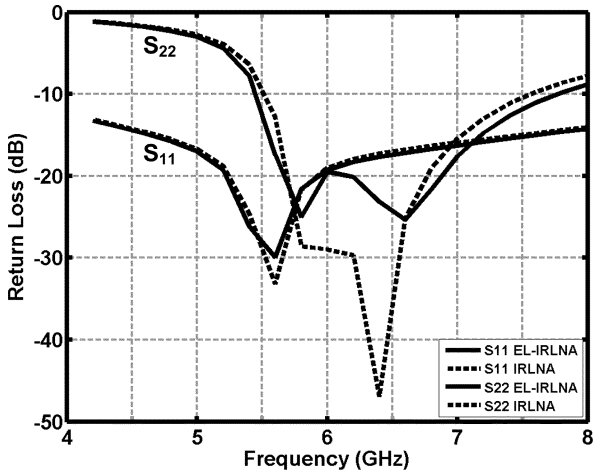

Fig. 13. Simulated return loss of EL-IRLNA and IRLNA.

end, the technique depicted in Fig. 10 is proposed to increase linearity wherein M_3 augments the bias current previously provided by M_1 only. With proper design, this topology remains more power efficient than a basic cascade amplifier because a significant fraction of the bias current is still reused.

There is a distinct tradeoff between additional bias current and linearity. Fig. 11 plots simulated IIP3 of the enhanced-linearity current reuse LNA (EL-IRLNA) as a function of additional bias current. Linearity improves as the additional bias current is increased, but eventually begins to saturate for large values. This is due to the increased voltage drop between the gate and source of M_2 with increased additional bias current; i.e., as $V_{gs,M2}$ is increased, the drain voltage of the CG stage is reduced, which leads to a reduced swing in the CG stage. Based on these simulations, the bias current through M_3 is chosen to be 2 mA, bringing the total current consumption to 3.5 mA. The simulated gain and noise figure characteristics of the EL-IRLNA and IRLNA circuits are plotted in Fig. 12 and the return losses are presented in Fig. 13. At a center frequency of 5.6 GHz, the IRLNA achieves a gain of 19 dB, while the EL-IRLNA achieves a gain of 20.3 dB. Both amplifiers achieve a 2.6 dB noise figure. Hence, for a supply current increase of 2 mA, the overall linearity is improved by about 6 dB.

VII. Measurement Results

The tuned-input tuned-output VCO (Fig. 3) and the g_m-boosted current-reuse LNA (Fig. 8) are fabricated in a six-metal 0.18 μm CMOS RF process. Both circuits are wafer probed on a Cascade probe station. Fig. 14 shows die microphotographs of the two circuits.

An on-chip differential amplifier buffer [2] is used in testing the VCO at a center frequency of 2.5 GHz. An Agilent E4446A spectrum analyzer with a phase noise personality is used for VCO measurements. Fig. 15 shows a measured tuning plot of the VCO wherein the oscillation frequency varies from 2.34 to 2.72 GHz as the control voltage $(V_{\rm ctl})$ changes from 0 to 2.5 V; the tuning range is 15.3%.

The measured phase noise spectral density (Fig. 16) of the VCO at 2.5 GHz is -110 dBc/Hz and -130.5 dBc/Hz at 100 kHz and 1 MHz offset frequencies, respectively. Beyond the offset frequency of 3 MHz, the measurement noise floor of the spectrum analyzer is approached and the measurement is no longer accurate. The spurs in the phase noise measurement are

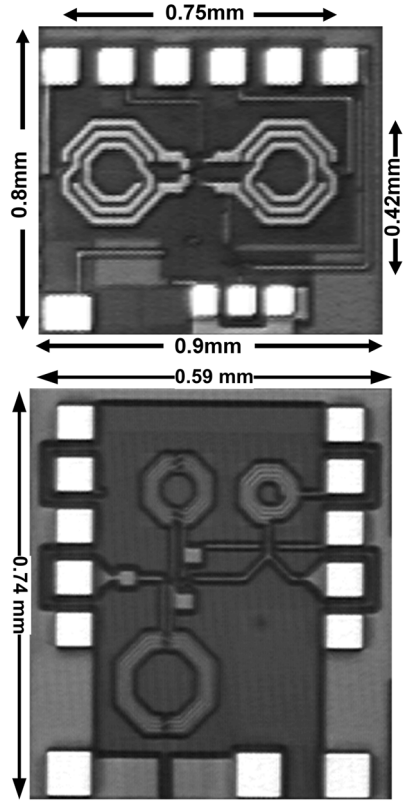

Fig. 14. Die microphotographs of the TITO VCO (top) and the g_m-boosted current-reuse LNA (bottom).

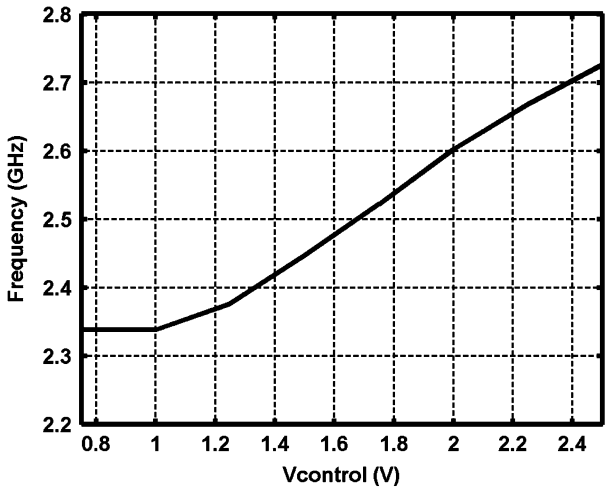

Fig. 15. Measured tuning range of the TITO VCO.

attributed to the measurement setup, and have been observed in the measurement of other VCOs in a similar setup [1].

A VCO figure-of-merit (FOM) is commonly defined as

$$\mathrm{FOM} = 10\log_{10}\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{L\{\Delta f\}P_{\mathrm{DC,mW}}}\right] \qquad (24)$$

where Δf is the offset frequency from the operating frequency, f_0, $L(\Delta f)$ is the phase noise power spectral density at this offset frequency, and $P_{\mathrm{DC,mW}}$ is the power dissipation in mW.

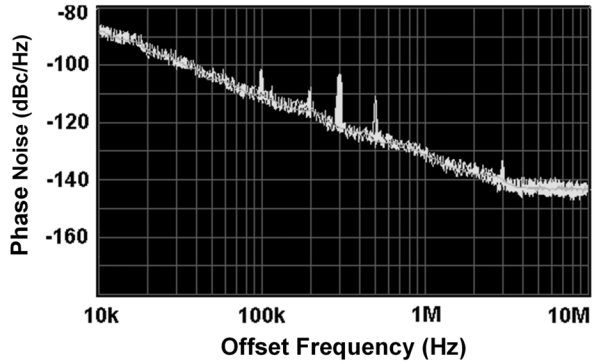

Fig. 16. Measured phase noise power spectral density of the TITO VCO at 2.5 GHz.

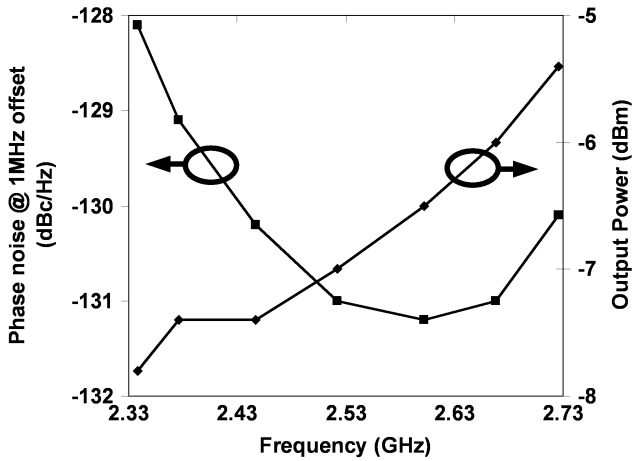

Fig. 17. Measured phase noise power spectral density at a 1 MHz offset frequency and the output signal power across the tuning range of the TITO VCO.

With a current consumption of 7.5 mA from a 1.8 V supply, and a tank Q of ~ 11, the CMOS TITO VCO achieves FOM $=$ 187.2 dBc/Hz.

Fig. 17 plots the measured phase noise spectral density of the VCO at 1 MHz offset across its tuning range. The output power level is also shown.

The gain (S_{21}) of the g_m-boosted current-reuse LNA varies as a function of bias conditions. The quality of the input match also depends on the bias current; hence, the gate voltage of the input CG stage is set to maintain reasonable $S_{11} < -10$ dB. The gate voltage of the output CS stage is set high enough to keep the CG stage in saturation. Measured S_{21} values for four different bias conditions vary from 14–21 dB as shown in Fig. 18. When biased for maximum and minimum gains, the LNA draws 1.5 and 0.8 mA, respectively, from a single 1.8 V power supply. The input match is maintained for the full-range of gain settings with $S_{11} < -10$ dB across the frequency band of operation. The measured input return loss and voltage gain for the maximum gain setting are plotted in Fig. 19. The noise figure (NF) of the LNA is measured using an Agilent N8975A Noise Figure Analyzer; it is shown for the maximum gain mode in Fig. 20. Finally, the measured OIP3 $= -2$ dBm characteristic is plotted for the high gain mode in Fig. 21.

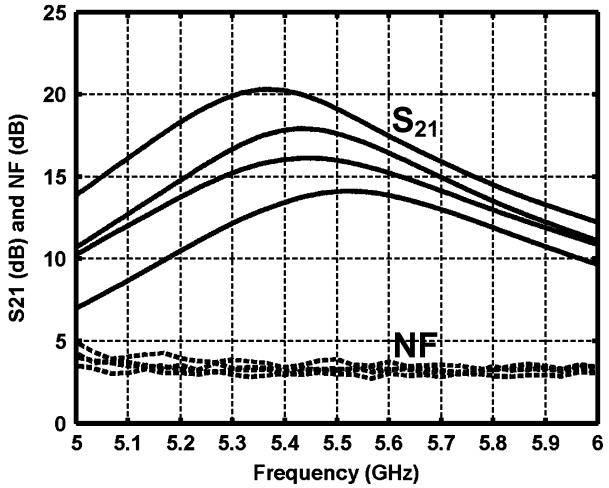

Fig. 18. IRLNA gains and noise figures measured for four different bias settings. Case 1 (topmost curve) is for maximum gain, and case 4 (lowest curve) is for minimum gain.

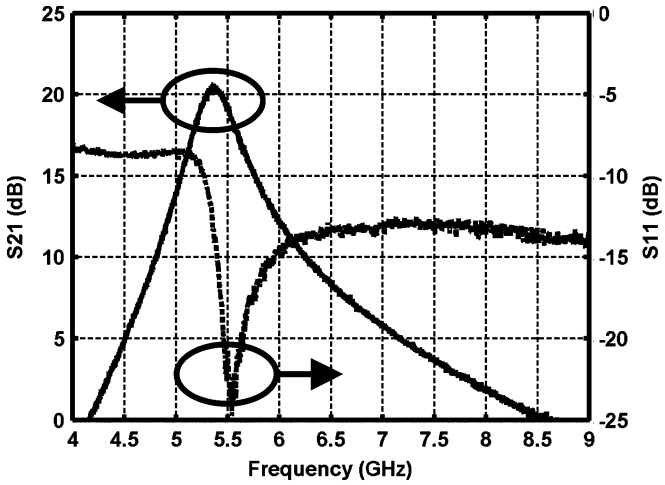

Fig. 19. Measured S_{21} and S_{11} for IRLNA in the maximum gain setting.

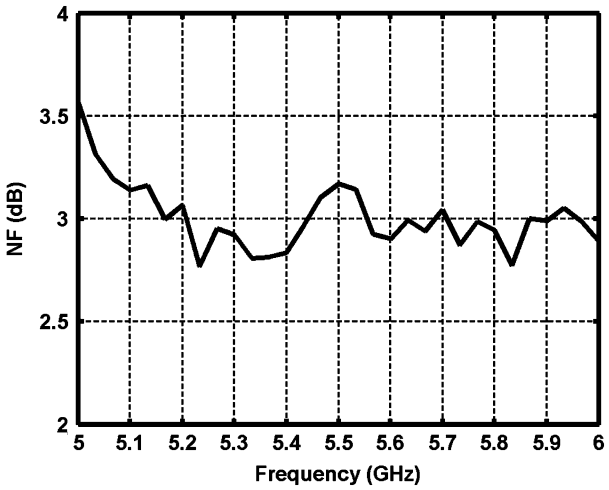

Fig. 20. Measured NF for IRLNA in the maximum gain setting.

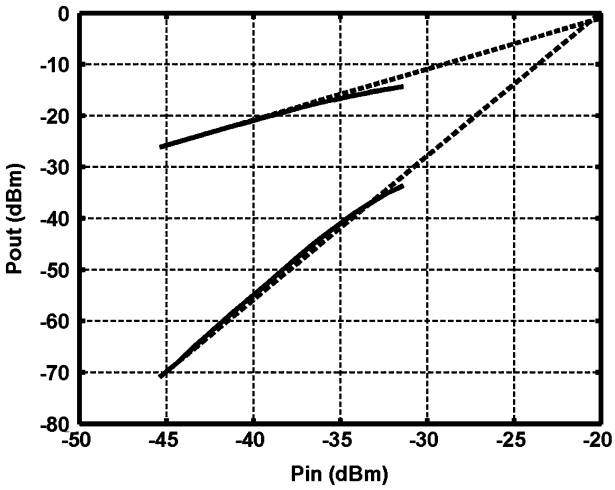

Fig. 21. Measured IM3 for IRLNA in the maximum gain setting.

VIII. Conclusion

A common-source amplifier can be configured as an oscillator or an LNA. Configured as an oscillator, a tuned-input tuned-output fully differential VCO in 0.18 μm CMOS is presented that has comparable tuning range and power consumption to cross-coupled VCOs, and superior phase noise performance. Hence, the TITO topology is an excellent design choice if phase noise is a key consideration, and the area overhead of an extra spiral inductor is tolerable. Configured as a common-source LNA, a current reuse g_m-boosted common-gate common-source cascaded LNA is presented that has comparable gain and noise performance to other high-gain LNAs with lower power consumption. It is an excellent design choice for low-power applications with somewhat relaxed linearity requirements. A modification to the LNA achieves enhanced linearity.

Appendix A

The frequency of oscillation and start-up condition for the TITO VCO with dissimilar tank circuits are derived by first calculating the admittances at the three nodes in Fig. 1

$$\mathbf{Y_f} = jB_f = j\omega C_f \tag{A-1}$$

$$\mathbf{Y_g} = G_g + jB_g = G_g + j\left(\omega C_g - \frac{1}{\omega L_g}\right) \tag{A-2}$$

$$\mathbf{Y_d} = G_d + jB_d = G_d + j\left(\omega C_d - \frac{1}{\omega L_d}\right). \tag{A-3}$$

Kirchhoff's phasor nodal equations yield [4]

$$(\mathbf{V_g} - \mathbf{V_d})\mathbf{Y_f} + \mathbf{V_g}\mathbf{Y_g} = 0 \tag{A-4}$$

$$(\mathbf{V_d} - \mathbf{V_g})\mathbf{Y_f} + \mathbf{V_d}\mathbf{Y_d} + g_m\mathbf{V_g} = 0. \tag{A-5}$$

Solving (A-4) and (A-5) gives

$$\mathbf{Y_f}\mathbf{Y_g} + \mathbf{Y_g}\mathbf{Y_d} + \mathbf{Y_d}\mathbf{Y_f} + g_m\mathbf{Y_f} = 0. \tag{A-6}$$

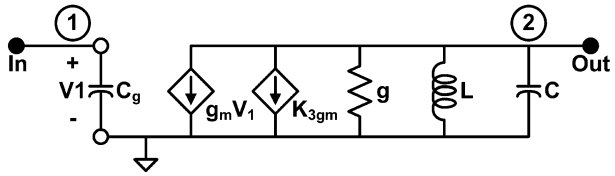

Fig. 22. Small-signal model for calculating third-order intermodulation distortion.

Considering the imaginary part of (A-6) and assuming the Q of the inductors is fairly high gives

$$\frac{1}{B_d}+\frac{1}{B_f}+\frac{1}{B_g}=\frac{G_dG_g}{B_dB_fB_g}\approx 0. \tag{A-7}$$

Thus, the reactive elements comprise a resonant loop at the frequency of oscillation. Hence, using (A-3), (A-5), and (A-7), the oscillation frequency is obtained as in (7). Considering the real part of (A-6)

$$\begin{aligned}-g_m &= G_d\left(1+\frac{B_g}{B_f}\right)+G_g\left(1+\frac{B_d}{B_f}\right)\\ &= G_d\left(1+\frac{C_g}{C_f}-\frac{1}{\omega^2L_gC_f}\right)\\ &\quad+G_g\left(1+\frac{C_d}{C_f}-\frac{1}{\omega^2L_dC_f}\right)\end{aligned} \tag{A-8}$$

which is the same as (9).

Appendix B

The linearity of a common-source amplifier with a tuned output is derived using Volterra analysis. First, the admittance matrix for the CS amplifier in Fig. 22 (ignoring K_{3gm}) is found to be

$$Y=\begin{bmatrix} sC_g & 0\\ g_m & \frac{1+sgL+s^2CL}{sL}\end{bmatrix}. \tag{B-1}$$

With the admittance matrix known, the first-order Volterra kernel, H_1, is found as

$$Y\cdot H=\mathrm{In} \tag{B-2}$$

$$\mathrm{In}=\begin{bmatrix}1\\0\end{bmatrix} \tag{B-3}$$

$$\begin{aligned}H_1&=\begin{bmatrix}\frac{1}{s_1C_g} & 0\\ -\frac{g_mL}{C_g\left(1+s_1gL+s_1^2CL\right)} & \frac{s_1L}{1+s_1gL+s_1^2CL}\end{bmatrix}\cdot\begin{bmatrix}1\\0\end{bmatrix}\\ &=\begin{bmatrix}\frac{1}{s_1C_g}\\ -\frac{g_mL}{C_g\left(1+s_1gL+s_1^2CL\right)}\end{bmatrix}=\begin{bmatrix}H_{11}\\H_{12}\end{bmatrix}.\end{aligned} \tag{B-4}$$

The matrix In represents the input stimulus, which is the voltage applied to the gate of the CS stage; H_{12} represents the linear transfer function of the system.

Next, the system of Fig. 22 is solved for the third-order response, this time with the gate shorted to ground and including K_{3gm}. The third-order Volterra kernel, H_3, is determined as shown in (B-5) and (B-6), at the bottom of the page. H_{32} represents the third-order transfer function of the system. The third-order intermodulation product, IM_3, is then calculated

$$\mathrm{IM}_3=\frac{3}{4}A^2\frac{H_{32}}{H_{12}}. \tag{B-7}$$

With $s_1=j\omega_1$, $s_2=j\omega_1$, and $s_3=-j\omega_2$, the third-order modulation term becomes (B-8), also shown at the bottom of the page. To simplify the calculation, the output inductor is assumed large, and the output capacitor is assumed small. This enables insight into the linearity as a function of the DC conditions as

$$\mathrm{IM}_3=\frac{3}{4}\frac{K_{3gm}}{g_m}\frac{1}{\omega_1\omega_2C_g^2}A^2. \tag{B-9}$$

Finally, to find the intercept point, A is determined for $IM_3=1$

$$A_{\mathrm{IP3}}=\sqrt{\frac{4}{3}\frac{g_m}{K_{3gm}}\omega_1\omega_2C_g^2} \tag{B-10}$$

which is the same result as seen in (23).

$$\mathrm{In}=\begin{bmatrix}0\\ \frac{K_{3gm}}{s_1s_2s_3C_g^3}\end{bmatrix} \tag{B-5}$$

$$\begin{aligned}H_3&=\begin{bmatrix}\frac{1}{sC_g} & 0\\ -\frac{g_mL}{C_g(1+sgL+s^2CL)} & \frac{sL}{1+sgL+s^2CL}\end{bmatrix}\cdot\begin{bmatrix}0\\ \frac{K_{3gm}}{s_1s_2s_3C_g^3}\end{bmatrix}\\ &=\begin{bmatrix}0\\ \frac{(s_1+s_2+s_3)LK_{3gm}}{\left(1+(s_1+s_2+s_3)gL+\left(s_1^2+s_2^2+s_3^2\right)CL+(s_1s_2+s_1s_3+s_2s_3)2CL\right)s_1s_2s_3C_g^3}\end{bmatrix}=\begin{bmatrix}H_{31}\\H_{32}\end{bmatrix}\end{aligned} \tag{B-6}$$

$$\begin{aligned}\mathrm{IM}_3&=\frac{3}{4}\frac{C_g}{g_mL}A^2\sqrt{\left(1-2\omega_1^2CL+\omega_1^2g^2L^2+\omega_1^4C^2L^2\right)}\\ &\times\sqrt{\frac{\left(-\omega_2+2\omega_1\right)^2L^2K_{3gm}^2}{C_g^6\omega_1^4\omega_2^2\left(1-\left(4\omega_1^2+\omega_2^2+4\omega_1\omega_2\right)2CL+\left(\omega_2^4+24\omega_1^2\omega_2^2-8\omega_2^3\omega_1+16\omega_1^4-32\omega_1^3\omega_2\right)(CL)^2+\left(4\omega_1^2-4\omega_1\omega_2+\omega_2^2\right)(gL)^2\right)}}\end{aligned} \tag{B-8}$$

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