Wideband CMOS Amplifier Design: Time-Domain Considerations

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Wideband CMOS Amplifier Design: Time-Domain Considerations

Jeffrey S. Walling, *Student Member, IEEE*, Sudip Shekhar, *Student Member, IEEE*, and David J. Allstot, *Fellow, IEEE*

***Abstract*—Time-domain responses of wideband CMOS amplifiers using several inductive peaking techniques are presented. Transient performance considerations are described, including the effects of transistor parasitics on settling and edge rates. A combination of time- and frequency-domain performance is derived for a given bandwidth extension technique, and tradeoffs are discussed. Measured results for several high-speed high-gain single-stage amplifiers are presented in 0.18-μm CMOS, and a design strategy for multistage amplifiers is introduced. Finally, design and simulation results are presented for a multistage amplifier in 0.18-μm CMOS that attains a bandwidth of 22.7 GHz with 14.7-dB voltage gain, operates at 40 Gb/s, and consumes 93.6 mW.**

***Index Terms*—Bandwidth extension, low power, peaking, setting time, T-coil, transformer, transient, wireline.**

I. Introduction

DESIGN techniques based on inductive peaking in CMOS amplifiers show that large increases in bandwidth are realized by exploiting capacitor-splitting and magnetic-coupling concepts. It is also shown that the optimum bandwidth extension ratio (BWER) is achieved by choosing the peaking technique based on the ratio of the effective drain capacitance of the driver device to its total load capacitance. Whereas Shekhar *et al.* [1] focus primarily on peaking techniques to maximize the −3-dB bandwidth of an amplifier, this paper details the time-domain characteristics associated with the peaking techniques and enables the choice of an optimum topology and design parameters that balance the frequency- and time-domain responses.

It is fundamental that the time- and frequency-domain responses of an amplifier are closely related, e.g., if the −3-dB bandwidth of its amplitude response is limited, it exhibits a slow response to a step input (i.e., a long rise time followed by a long exponential settling tail). Thus, in a digital data transmission application, an input bit stream suffers intersymbol interference (ISI) that manifests on the output eye diagram as a reduced voltage margin. The time-domain step response needs small ringing and fast settling for low ISI. The timing margin is also compromised because jitter is exacerbated by slower edge rates [2]. For these reasons, a large −3-dB bandwidth is generally needed. In optical and wireless applications where pulse fidelity is important, a linear phase response is also desirable. A measure of linearity of the phase response is the group delay of the signal, i.e., linear phase means constant group delay. A good group delay characteristic in the frequency domain is, in turn, related to low overshoot in the step response in the time domain.

Classical amplifier design techniques have focused on attaining a certain kind of response, e.g., a Bessel filter response, which has a good group delay characteristic at the cost of a longer rise time. A Butterworth filter has a maximally flat amplitude response but large overshoot and poor settling in its step response. Current needs call for a design technique that makes a good compromise between the amplitude and phase (or group delay) responses in the frequency domain, or between the rise-time and overshoot/ringing in the time domain. Furthermore, the classical filter design techniques achieve these responses with a large number of inductors, which makes them less attractive for CMOS implementations. Inductive peaking techniques like shunt peaking and shunt-series peaking are simple to implement and enable a good tradeoff. However, further improvements in performance can be attained through techniques like bridged-shunt peaking, bridged-shunt-series peaking, asymmetric T-coil peaking, etc. [1].

In order to obtain the best eye in digital data transmission applications, both eye height and width are important. The design procedure should also aim for maximum bandwidth [1]. However, as shown later, an amplifier optimized for maximum −3-dB bandwidth may not perform optimally in terms of group delay or overshoot/ringing. Hence, a two-step design procedure is proposed. First, the bandwidth of the amplifier should be maximized, and then optimization should be performed to obtain an acceptable phase response at the probable cost of some loss in bandwidth.

Several inductive peaking techniques that improve the bandwidth and rise-time of a single-stage CMOS amplifier are briefly reviewed in Section II. The underlying theoretical formulations are derived treating the driver transistor as a simple voltage-dependent current source in shunt with a capacitance C_1, which represents the effective total parasitic capacitance at the nMOS drain node. Next, the effects of important nonidealities gate-to-drain overlap capacitance $(C_{\rm gd})$ and small-signal output drain-to-source conductance $(g_{\rm ds})$ are described in Section III. Section IV gives experimental results for several inductively-peaked single-stage amplifiers in 0.18-μm CMOS. Finally, Section V presents a design methodology for multistage amplifiers and simulation results for a multistage design in 0.18-μm CMOS.

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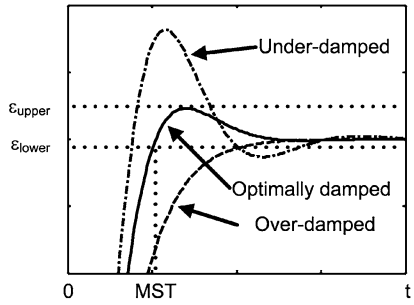

Fig. 1. Settling time definition where MST denotes minimum settling time.

II. Inductive-Peaking Techniques

Peaking techniques to improve the bandwidth and rise-time of single-stage amplifiers are due to Wheeler [3] and Muller [4]; those germane to oscilloscope design are summarized by Hofer [5], and those addressing CMOS wideband amplifier design are described by Lee [6]. Various other peaking techniques are also known [1], [7]–[9]. The basic approaches can be classified on the basis of the number of spirals they employ: single inductor (e.g., shunt, bridged-shunt, or series), double-inductor (e.g., shunt-series or bridged shunt-series), and transformer (e.g., symmetric T-coil and asymmetric T-coil).

A brief overview of peaking methods comparing their step responses is presented to gain insight into their most appropriate use. For normalization purposes, the peaking techniques are compared to an unpeaked one-pole reference amplifier with unity dc gain and -3-dB bandwidth ($f_0 = 1$ Hz). Settling time takes the usual definition as the time at which the amplifier settles to within a specified error bounds and after which does not leave it. Yang *et al.* [10] show that, in order to obtain the theoretical minimum settling time (MST) for a second-order system, the step response should equal but not exceed the specified upper error bound on the first peak of the overshoot. Fig. 1 depicts the differences in settling times for a second-order system with three different damping factors. Although an under-damped system clearly has a faster rise time, it can take longer to settle to its final value, due to excessive overshoot, than an over-damped system. Of course, high-order systems behave differently than second-order systems, but it is generally true that, if the overshoot of the first or second peak is optimized, the system achieves MST. An error bound of $\varepsilon = 2\%$ is assumed unless otherwise indicated [11], and various techniques are compared using the settling time reduction ratio (STRR), defined as

$$\mathrm{STRR} = \frac{\tau_{s,\mathrm{ref}}}{\tau_{s,\mathrm{peak}}}. \tag{1}$$

STRR compares the settling times of the reference $(\tau_{s,\mathrm{ref}})$ and peaked $(\tau_{s,\mathrm{peak}})$ amplifiers. Thus, a large STRR (> 1) is desirable.

Rise time, τ_r, is defined as the time for the output of the amplifier to rise from 10% to 90% of its final value. Another useful metric is the rise time reduction ratio (RTRR)

$$\mathrm{RTRR} = \frac{\tau_{r,\mathrm{ref}}}{\tau_{r,\mathrm{peak}}}. \tag{2}$$

It compares the rise times of the reference $(\tau_{r,\mathrm{ref}})$ and peaked $(\tau_{r,\mathrm{peak}})$ amplifiers. A large RTRR (> 1) is desirable.

One general conclusion of this work is that the maximum values of BWER, STRR and RTRR are not simultaneously attainable; hence, design tradeoffs must be made among the various peaking techniques to attain an optimum response for a given application.

A. Single-Inductor Peaking

Consider the shunt-peaked amplifier in Fig. 2(a) where R, C_1, C_2, and L represent the load resistance, drain capacitance, load capacitance, and the shunt inductance, respectively; $C = C_1 + C_2$ is the total load capacitance.

Voltage gain is the product of the impedance $Z(s)$ of the load network, and the small-signal transconductance of the driver transistor, g_m. For the shunt-peaked amplifier, we have

$$A_V(s) = -g_m \frac{R + sL}{1 + sRC + s^2LC}. \tag{3}$$

The small-signal -3-dB bandwidth is increased because of the transmission zero introduced by the inductor, i.e., as frequency increases, the impedance of the load network increases to compensate for decreases in the impedance of C. Substituting $\omega_0 = 1/RC$ and the time constant ratio $m = R^2C/L$ into (3) gives

$$A_V(s) = -g_m R \frac{(1 + s/m\omega_0)}{1 + s/\omega_0 + s^2/m\omega_0^2}. \tag{4}$$

It is well known that the maximum BWER for the simple shunt-peaked network is 1.84 for $m = 1.414$ [5], [6], but this BWER is accompanied by 1.5 dB of peaking in the amplitude response. Peaking is usually undesirable, but, in some applications (e.g., high-speed interconnects), it is used as a basis for continuous-time linear equalization of the channel loss.

In shunt-peaked applications where a flat frequency response is desired, 0 dB of peaking is achieved with a BWER of 1.72 for $m = 2.414$. A higher BWER is obtained by shunting inductor L with capacitor C_B to form the bridged-shunt-peaked network of Fig. 2(b) [3], [4]. The bridge capacitance is sufficiently large to negate peaking but sufficiently small to not significantly reduce the bandwidth.

Introducing a variable $k_B = C_B/C$, the small-signal voltage gain of the bridged-shunt-peaked amplifier is [1]

$$A_V(s) = -g_m R \frac{1 + \left(\frac{1}{m}\right)\frac{s}{\omega_0} + \left(\frac{k_B}{m}\right)\frac{s^2}{\omega_0^2}}{1 + \frac{s}{\omega_0} + \left(\frac{k_B+1}{m}\right)\frac{s^2}{\omega_0^2} + \left(\frac{k_B}{m}\right)\frac{s^3}{\omega_0^3}}. \tag{5}$$

Step and group delay responses of shunt-peaked $(k_B = 0.0)$, bridged-shunt peaked, and unpeaked reference amplifiers are compared in Fig. 3. The bridged-shunt peaked amplifier with similar BWER (~ 1.83) as the shunt-peaked design provides a significant settling time improvement; it achieves $\mathrm{STRR} = 1.3$ whereas the shunt-peaked amplifier settles slower than the reference design owing to excessive overshoot and ringing. It is interesting to note, however, that if settling time is more important than bandwidth enhancement, an STRR of 2.13 can be achieved in a bridged-shunt peaked amplifier for $k_B = 0.1$ and $m = 2.84$ with $\mathrm{BWER} = 1.69$. Another conclusion illustrated in Fig. 3

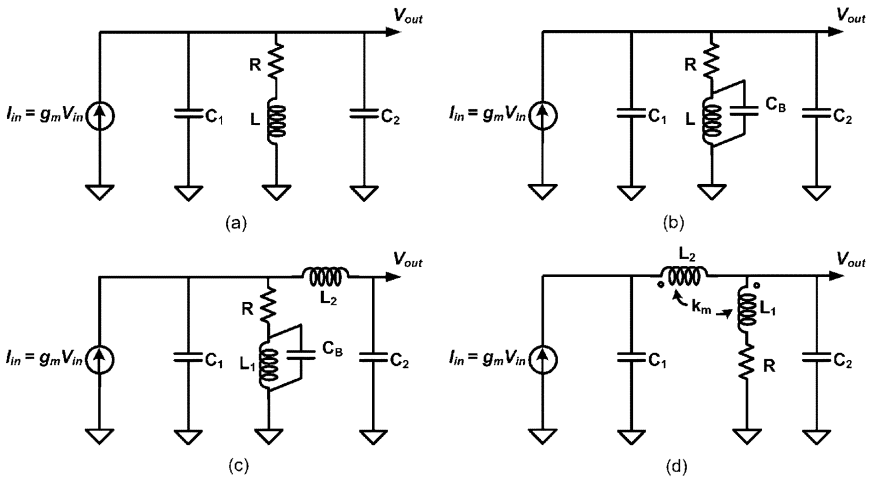

Fig. 2. Equivalent circuit schematics of (a) shunt-peaked, (b) bridged-shunt-peaked, (c) bridged-shunt-series-peaked and (d) asymmetric T-coil peaked amplifiers.

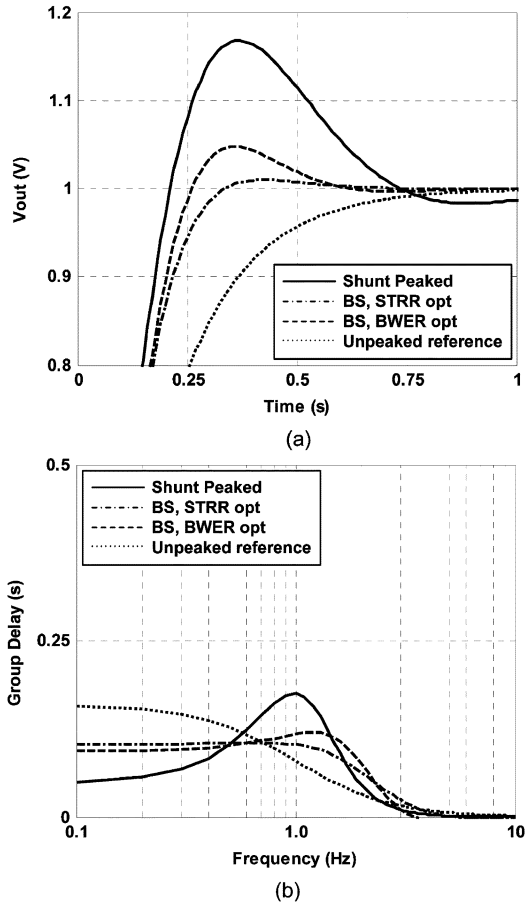

Fig. 3. Normalized (a) time-domain step responses and (b) frequency-domain group delay responses of the shunt-peaked, bridge-shunt-peaked (BS), and unpeaked reference amplifiers.

is that a large STRR generally corresponds to a flat group delay response. Thus, if a good settling characteristic is needed, an optimization for group delay, not maximum bandwidth, should yield such a response. Reduction in rise time compared with the reference amplifier is similar for both peaking techniques with

TABLE I
PERFORMANCE OF SHUNT-PEAKED ($k_B = 0.0$) AND BRIDGED-SHUNT-PEAKED AMPLIFIERS

k_B	m	STRR	RTRR	BWER
0.0	1.4	0.93 ± 0.01	2.14 ± 0.01	1.85 ± 0.01
0.1	*2.84*	*2.13 ± 0.02*	*1.68 ± 0.02*	*1.69 ± 0.01*
0.3	2.4	1.27 ± 0.02	1.88 ± 0.01	1.85 ± 0.01

an optimum $\mathrm{RTRR} = 2.14$ obtained with shunt-peaking. Several shunt- and bridged-shunt-peaked frequency- and time-domain responses are compared in Table I. The response optimized for STRR is highlighted in italics.

In practice, any CMOS shunt-peaked amplifier that uses on-chip spiral inductors has some degree of bridging due to parasitic capacitance. If greater bridging is desired, additional capacitance is added in parallel with the parasitic. Another advantage of the bridged-shunt network is that it achieves maximum BWER or STRR for a larger value of m, which manifests as smaller on-chip inductors. Because component tolerances are always a concern when passive networks are used, 95% confidence intervals are added to the STRR, RTRR, and BWER values in Table I to give an estimate of the sensitivities to variations. The confidence intervals are obtained from 100 000-point Monte Carlo simulations with the following component distributions that are assumed throughout this paper; capacitances and inductances have Gaussian distributions with standard deviations of $\sigma = 10\%$ and $\sigma = 5\%$, respectively.

Eye diagrams of two bridged-shunt-peaked amplifiers optimized for maximum BWER ($k_B = 0.1$, $m = 2.84$) and maximum STRR ($k_B = 0.3$, $m = 2.4$) are shown in Fig. 4(a) and (b), respectively. The eye diagrams are simulated using a random pattern generator with a periodicity of $2^{31} - 2$, and the generated random sequence had a length of 2^{12}. The data rate used in the simulations is 4.8 times the −3-dB bandwidth of the unpeaked reference amplifier, which corresponds to 2.0 times the bandwidth of the STRR optimized amplifier

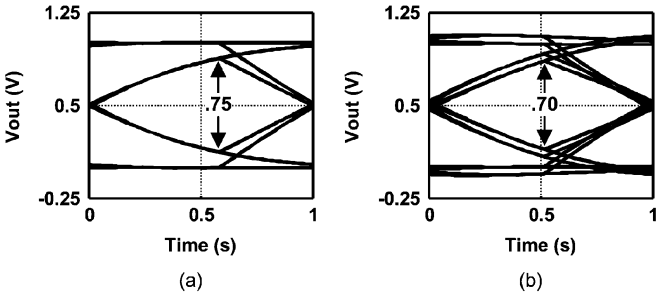

Fig. 4. Eye diagrams for bridged-shunt-peaked amplifiers optimized for (a) fast settling with $k_B = 0.1$, $m = 2.84$, and (b) maximum bandwidth with $k_B = 0.3$, $m = 2.4$. The data rate is 4.8 times $f_{-3\,\mathrm{dB}}$ of the reference amplifier.

and 1.7 times the bandwidth of the BWER optimized amplifier. The eye opening (both horizontal and vertical) of the maximum STRR design is better than for the maximum BWER case.

B. Double-Inductor Peaking

In cases where the effective drain parasitic capacitance of the driver device is comparable to its extrinsic load capacitance, larger bandwidth extension is achieved using *capacitor-splitting* wherein a series inductor physically separates C_1 and C_2 [Fig. 2(c)]. The inductor L_2 delays current flow to C_2 so that initially only C_1 is charged or discharged.

As C_1 is only a fraction of the total load capacitance, C, the effective rise and fall times at the drain are reduced substantially. This method is known generally as series peaking. Combining it with the shunt-peaking techniques described above results in the shunt-series [7], [12] and bridged-shunt-series-peaked topologies [Fig. 2(c)] [1], [3], [4].

Substituting $m_1 = R^2C/L_1$, $m_2 = R^2C/L_2$, $k_C = C_1/C$, $k_B = C_B/C$, and $\omega_0 = 1/RC$, the small-signal gain of the bridged-shunt-series-peaked amplifier is shown in (6) [1], at the bottom of the page.

A maximum BWER of 4 with 2 dB of peaking is obtained for $k_C = 0.4$, $k_B = 0.2$, $m_1 = 6$, and $m_2 = 2.4$; however, the increased bandwidth comes at the cost of time-domain performance—a settling time $(\mathrm{STRR} = 1.0)$ equal to the unpeaked reference design $(\mathrm{STRR} = 1.0)$. A BWER of 3.92 with 0 dB of peaking is achieved for $k_C = 0.4$, $k_B = 0.3$, $m_1 = 8$, and $m_2 = 2.4$; however, STRR is 1.06, which is only slightly faster than the reference design. Instead, if the time-domain response is optimized with $k_C = 0.4$, $k_B = 0.1$, $m_1 = 5.5$, and $m_2 = 1.7$, STRR is improved to 1.43 with a BWER of 2.84. From Fig. 5 it is again clear that a larger STRR corresponds to a flatter group delay response. Several step responses for shunt-series- and bridged-shunt-series-peaked amplifiers are

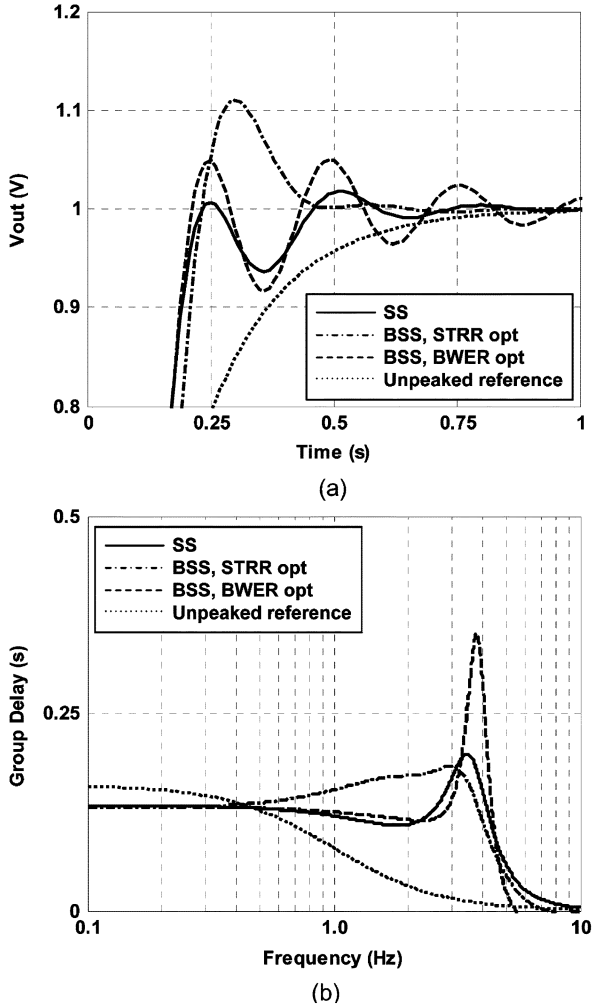

Fig. 5. Normalized (a) time-domain step responses and (b) frequency-domain group delay responses of shunt-series-peaked (SS), bridged-shunt-series-peaked (BSS), and unpeaked reference amplifiers.

shown in Fig. 5 and summarized in Table II. The designs optimized for STRR and BWER are highlighted in italics. Again, 100 000-sample Monte-Carlo-based 95% confidence intervals are added to the tabulated STRR, RTRR, and BWER values.

The bridged-shunt-series-peaked topology is optimal for larger capacitance ratios (e.g., $k_c > 0.4$). Its BWER is considerably higher than bridged-shunt peaking as evidenced by the faster edge rates in Fig. 5 compared with Fig. 3. It is evident that there are unavoidable tradeoffs among STRR, RTRR, BWER, and chip area.

The eye diagrams of two bridged-shunt-series-peaked-amplifiers optimized for maximum STRR $(k_C = 0.4, k_B = 0.1, m_1 = 5.5, m_2 = 1.7)$ and maximum BWER $(k_C = 0.4,$

$$A_v(s) = -g_m R \frac{1 + \left(\frac{1}{m_1}\right)\frac{s}{\omega_0} + \left(\frac{k_m}{m_1}\right)\frac{s^2}{\omega_0^2}}{1 + \frac{s}{\omega_0} + \left(\frac{1+k_B}{m_1} + \frac{1-k_C}{m_2}\right)\frac{s^2}{\omega_0^2} + \left(\frac{k_B}{m_1} + \frac{k_C(1-k_C)}{m_2}\right)\frac{s^3}{\omega_0^3} + \left(\frac{(k_C+k_B)(1-k_C)}{m_1 m_2}\right)\frac{s^4}{\omega_0^4} + \left(\frac{k_B k_C(1-k_C)}{m_1 m_2}\right)\frac{s^5}{\omega_0^5}} \tag{6}$$

TABLE II
PERFORMANCE OF SHUNT-SERIES-PEAKED ($k_B = 0.0$) AND BRIDGED-SHUNT-SERIES-PEAKED AMPLIFIERS

k_C	k_B	m_1	m_2	STRR	RTRR	BWER
0.4	0.0	6.3	2.6	1.43 ± 0.04	2.17 ± 0.02	3.47 ± 0.12
	0.1	5.5	1.7	1.43 ± 0.09	2.05 ± 0.03	2.84 ± 0.10
	0.2	6	2.4	1.00 ± 0.03	2.27 ± 0.01	4.01 ± 0.05
	0.3	8	2.4	1.06 ± 0.18	2.77 ± 0.01	3.94 ± 0.09
0.5	0.1	6	2	0.87 ± 0.19	2.31 ± 0.01	3.41 ± 0.04
	0.2	6	2	0.90 ± 0.15	2.34 ± 0.01	3.55 ± 0.03

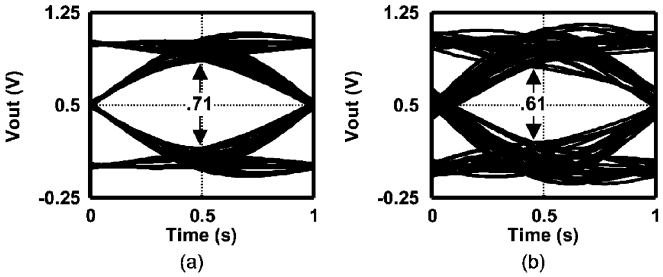

Fig. 6. Eye diagrams for bridged-shunt-series-peaked amplifiers optimized for (a) fast settling with $k_C = 0.4k_B = 0.1$, and (b) maximum bandwidth with $k_C = 0.4$, $k_B = 0.2$. The data rate is 6.6 times the $f_{-3\,\mathrm{dB}}$ of the reference amplifier.

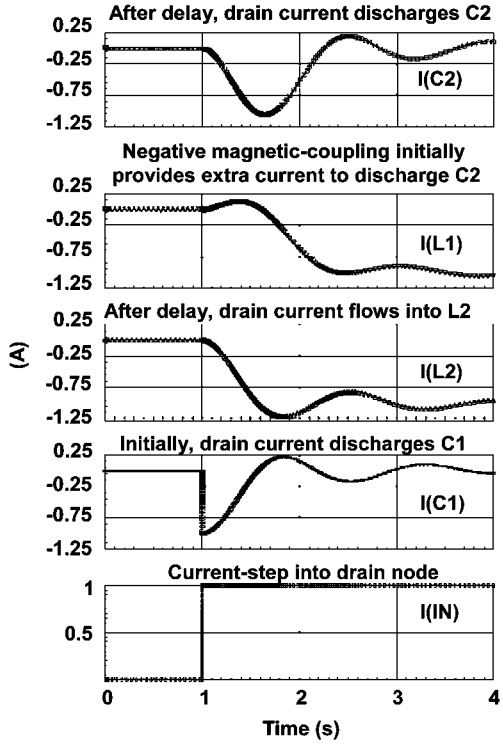

Fig. 7. Transient responses at different nodes of a T-coil-peaking network to a step input.

$k_B = 0.2$, $m_1 = 6.0$, $m_2 = 2.4$) are compared in Fig. 6. The data rate used in the simulations is 6.6 times the −3 dB bandwidth of the un-peaked reference amplifier, which corresponds to 2.3 (1.6) times the bandwidth of the STRR- (BWER-) optimized amplifier. Similar to the results for the bridged-shunt peaked amplifier, the eye opening (both horizontal and vertical) of the maximum STRR design is better than for the maximum BWER case.

C. Transformer Peaking

Another attractive peaking technique in terms of die area and BWER uses asymmetric T-coils to provide bandwidth extension [1], [9], [13] [Fig. 2(d)]. T-coil designs are advantageous when the drain parasitic capacitance is small compared with the total load capacitance; i.e., $0.1 < k_c < 0.4$.

To gain insight into the functionality of the circuit, consider the step response of the amplifier as shown in Fig. 7. The secondary inductor L_2 splits capacitors C_1 and C_2 so that the drain current flows initially only through C_1. After that, the current flows through L_2 which causes a proportional current flow through C_2. Finally, the negative magnetic coupling boosts the amount of current that flows initially through C_2 because it is effectively connected in series with the negative mutual inductance, $-M$. From this description, it is evident that the asymmetric T-coil technique is actually an extension of its double-series-shunt counterpart.

Substituting the coupling coefficient $k_m = M/(L_1L_2)^{1/2}$ and m_1, m_2, k_c, and ω_0 as defined above, the small-signal voltage gain transfer function of the asymmetric T-coil amplifier is as given in (7) [1], shown at the bottom of the page.

A significant advantage of the asymmetric T-coil-peaked amplifier is its larger BWER (e.g., $\mathrm{BWER} = 5.61$ with 2 dB of peaking) compared with the bridged-shunt-series-peaked design (e.g., $\mathrm{BWER} = 4$ for 2 dB of peaking); however, due to the peaking in the response, there is substantial ringing and STRR is only 1.69. In the case of 0-dB peaking, it still offers a substantial advantage (e.g., $\mathrm{BWER} = 4.66$ versus $\mathrm{BWER} = 3.94$), but this offers an STRR of 3.34.

The 0-dB peaked design has some sensitivity due to PVT, and, if a more robust design for STRR is desired, an optimization in the time domain rather than in the frequency domain yields an STRR of 3.26 with a BWER of 3.35. The normalized time-domain step responses for two asymmetric T-coil-peaked amplifiers are compared to the unpeaked reference design in Fig. 8

$$A_v(s) = -g_m R \frac{1 + \left(\frac{1}{m_1} + \frac{k_m}{\sqrt{m_1 m_2}}\right)\frac{s}{\omega_0}}{1 + \frac{s}{\omega_0} + \left(\frac{1}{m_1} + \frac{k_C}{m_2} + \frac{2k_C k_m}{\sqrt{m_1 m_2}}\right)\frac{s^2}{\omega_0^2} + \left(\frac{k_C(1-k_C)}{m_2}\right)\frac{s^3}{\omega_0^3} + \left(\frac{k_C(1-k_C)(1-k_m^2)}{m_1 m_2}\right)\frac{s^4}{\omega_0^4}} \tag{7}$$

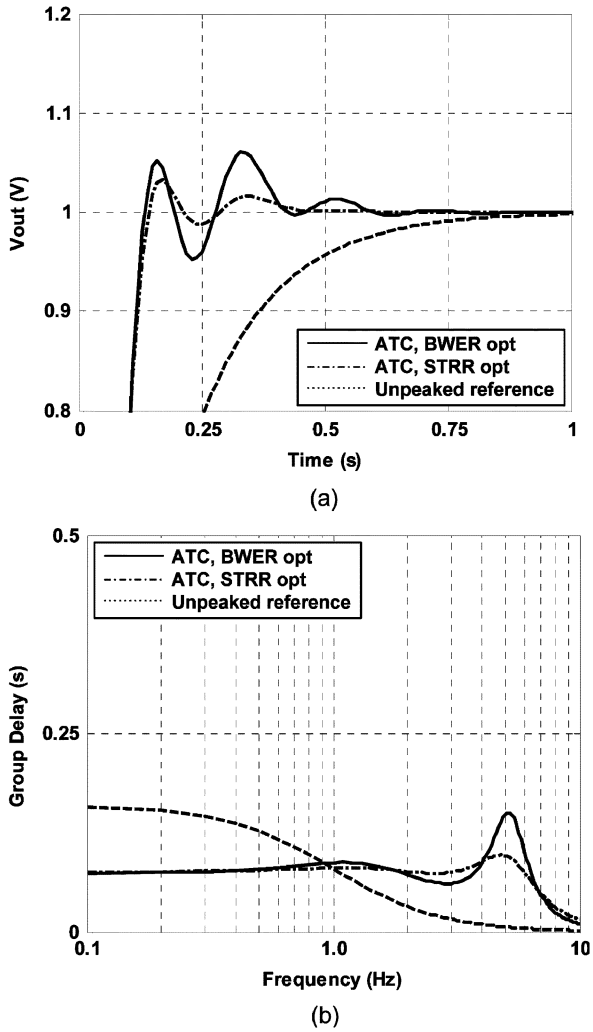

Fig. 8. Normalized (a) time-domain step responses and (b) frequency-domain group delay responses of two asymmetric T-coil peaked (ATC) amplifiers and the unpeaked reference design.

TABLE III
PERFORMANCE IN ASYMMETRIC T-COIL-PEAKED AMPLIFIERS

k_C	k_m	m_1	m_2	STRR	RTRR	BWER
0.1	0.7	4.0	1.6	3.34 ± 0.36	2.42 ± 0.03	4.66 ± 0.19
	0.6	3.5	1.6	1.69 ± 0.08	2.33 ± 0.04	5.61 ± 0.10
	0.6	*4.1*	*2.8*	*1.97 ± 0.1*	*1.62 ± 0.04*	*2.27 ± 0.04*
	0.7	*4.1*	*1.5*	*3.30 ± 0.21*	*2.42 ± 0.03*	*4.68 ± 0.14*
0.2	0.6	5.5	2.4	1.69 ± 0.01	2.15 ± 0.02	4.15 ± 0.10
	0.6	3.0	2.0	1.26 ± 0.02	2.42 ± 0.01	4.52 ± 0.14
	0.6	*4.3*	*2.1*	*2.58 ± 0.55*	*2.30 ± 0.01*	*4.09 ± 0.12*
	0.7	*4.6*	*2.2*	*3.26 ± 0.03*	*2.25 ± 0.01*	*3.35 ± 0.08*
0.3	0.5	4.0	2.8	1.38 ± 0.02	2.22 ± 0.01	3.94 ± 0.35
	0.4	4.0	2.8	1.38 ± 0.01	2.27 ± 0.01	4.56 ± 0.07
	0.6	*5.6*	*2.4*	*3.20 ± 0.01*	*2.20 ± 0.01*	*3.21 ± 0.08*
	0.6	*4.8*	*2.6*	*3.19 ± 0.01*	*2.19 ± 0.01*	*3.04 ± 0.09*

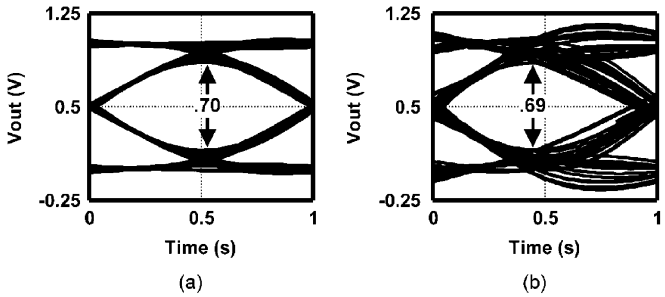

Fig. 9. Eye diagrams for asymmetric T-coil-peaked amplifiers optimized for (a) fast settling ($k_m = 0.7$, $m_1 = 4.0$, and $m_2 = 1.6$) and (b) maximum bandwidth ($k_m = 0.6$, $m_1 = 3.5$, and $m_2 = 1.6$). The data rate is 10.6 times $f_{-3\text{ dB}}$ of the reference amplifier.

and the results are summarized in Table III. The amplifiers optimized for STRR are highlighted in italics. Again, the amplifier with the fastest settling time corresponds to the one with the flattest group delay across the band. It should be noted that when optimizing for STRR, if the amplifier is designed so that the first peak overshoot just touches the upper edge of the settling boundary, the design can exhibit a bimodal performance distribution versus PVT variations. This effect is evident in the seventh row of Table III where the confidence interval is unusually large. Note that there are many other design options that do not show such a large variance.

The eye diagrams of two asymmetric T-coil peaked amplifiers optimized for maximum STRR ($k_C = 0.1$, $k_m = 0.7$, $m_1 = 4.0$, and $m_2 = 1.6$) and maximum BWER ($k_C = 0.1$, $k_m = 0.6$, $m_1 = 3.5$, and $m_2 = 1.6$) are compared in Fig. 9. The data rate used in the simulation is 10.6 times the -3-dB bandwidth of the unpeaked reference amplifier, which corresponds to 2.3 (1.9) times the bandwidth of the STRR- (BWER-) optimized amplifier. Again for the asymmetric T-coil peaked amplifier, the eye opening (both horizontal and vertical) of the maximum STRR design is better than for the maximum BWER case.

Compared with a bridged-shunt-series peaked amplifier, a T-coil peaked design provides higher RTRR, BWER and STRR values with a smaller chip area. A tradeoff is that the design of the T-coil adds complexity to the overall synthesis.

D. Optimization

To this point, several peaking techniques have been presented, representing a good sample of the design space for inductively peaked wideband amplifiers. It has also been shown that the choice of an optimum peaking technique is dependent on the physical properties of the amplifier (e.g., k_c) and its desired performance for BWER, RTRR, and STRR.

In the case of the shunt-peaked amplifier, the design choices can be made analytically to find the damping and natural frequency of the system, because it has a second-order response. However, for other peaking techniques, the complexity of the system increases, with a cubic, quartic and quintic response for the bridged-shunt, the asymmetric T-coil and bridged-shunt-series peaking, respectively. These equations are solvable using computational software, but the results are unwieldy and do not enable insight into improving either the bandwidth or settling behavior of the system. To this end, an optimization strategy is useful for finding the best design choices for enhancing the frequency- and time-domain performance of the inductively-

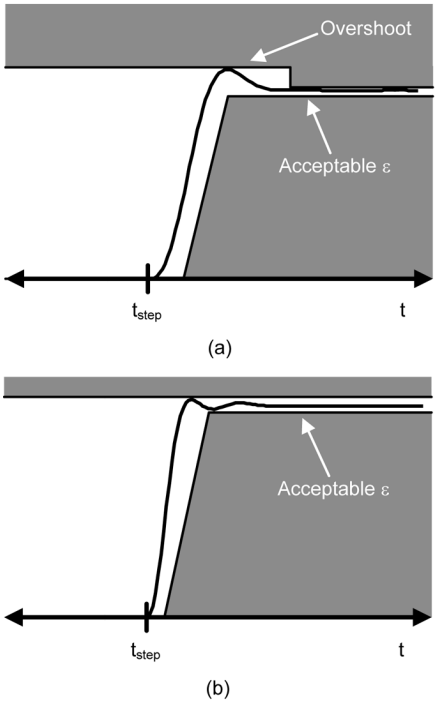

Fig. 10. Optimization constraints for minimizing settling time in wideband amplifiers (a) with and (b) without overshoot.

peaked amplifiers. A graph-based approach to obtaining optimal component values in the design space is chosen using the MATLAB optimization toolbox. For the present purposes, only time-domain optimization is considered, but it should be noted that frequency-domain optimization proceeds in a similar manner.

Optimization is performed for two different scenarios (Fig. 10) to insure that the true minimum settling time of the amplifier is found. Fig. 10(a) represents an amplifier that is allowed to overshoot the desired settling window, and then settle quickly after the overshoot, whereas (b) depicts the condition where the amplifier response is allowed to just touch the upper error bound before settling to its final value.

Optimization proceeds by first fixing the value of k_c, as it will be known for a given gain and load condition. Next, a pattern search using a genetic algorithm optimizes the other parameters (k_b, k_m, m_1, m_2, etc.) until an acceptable value of STRR, BWER, etc., is found. The error bounds are then tightened until no improvement is seen in the amplifier performance.

E. Summary

Several important conclusions are drawn from the comparisons above. First, the choice of an optimal peaking technique depends on the ratio of total effective drain parasitic capacitance, C_1, to the total load capacitance, C. When this ratio is small ($0.1 < k_C < 0.4$), the edge-rate requirements are relaxed and simplicity of design is a necessity, the shunt-peaked or bridged-shunt peaked approach is preferred, with the final choice dependent upon the application details. When k_C is small and fast edge-rates are required, the asymmetric T-coil-peaked approach is advantageous. The bridged-shunt-series-peaked amplifier is optimal in cases where k_C is large ($k_C > 0.4$). In general, the asymmetric T-coil peaked amplifier is able to simultaneously achieve good BWER and STRR, whereas the shunt-peaked and bridged-shunt-series-peaked amplifiers require prudent tradeoffs. As a rule, in order to achieve the best performance in both the time and frequency domains, a two-pronged optimization should be performed. The first optimization should be done to achieve the desired bandwidth, followed by an optimization to fine tune the time-domain performance. A summary of various peaking techniques with their optimum regions of operation is given in Table IV.

Applications of different peaking techniques for $k_C < 0.5$ have been described. With $k_C > 0.5$ (i.e., $C_2 < C_1$), however, the position of L_2 with respect to C_1 and C_2 should be interchanged based on the principal of reciprocal networks [4] to synthesize the optimum bridged-shunt-series-peaked and asymmetric T-coil-peaked networks.

III. Effects of Other Device Parasitics

In most applications, it is desirable to obtain the overall voltage gain in as few stages as possible in order to minimize power consumption, chip area and the bandwidth shrinkage effects characteristic of multistage amplifiers. This adds complexity to the design of the gain stage, however, as the driver device is necessarily wide to obtain large gain, which leads to increased parasitic effects [14]. If the parasitics of M_1 are ignored, ideal gain expressions [e.g., (1) and (2)] are obtained. An increase in the dc gain ($A_{V0} = g_m R$) is achieved by increasing the device width to increase g_m, but this causes deleterious increases in the $C_{\rm gd}$ and $g_{\rm ds}$ parasitics. For better insight into this case, the common-source shunt-peaked amplifier should include the parasitic components $C_{\rm gd}$ and $g_{\rm ds}$ of the driver device M_1, as shown in Fig. 11.

A. Effects of $C_{\rm gd}$

Including $C_{\rm gd}$, the voltage gain of the shunt-peaked amplifier (Fig. 11) is

$$A_v(s) = \frac{(sC_{\rm gd} - g_m).(R + sL)}{s^2 L(C + C_{\rm gd}) + sR(C + C_{\rm gd}) + 1}. \tag{8}$$

Thus, $C_{\rm gd}$ introduces a right-half-plane (RHP) zero that degrades the settling response. Introducing the variable $k_p = C_{\rm gd}/(C_{\rm gd} + C)$ with $\omega_z = g_m/C_{\rm gd}$ into (8) gives

$$A_V(s) = -g_m R \frac{\left(1 - \frac{s}{\omega_z}\right)\left(1 + \frac{s}{m\omega_0}\right)}{1 + \frac{s}{\omega(1-k_p)} + \frac{s^2}{m\omega_0(1-k_p)}}. \tag{9}$$

From (9), the RHP zero is at a very high frequency for a small $C_{\rm gd}$ and has little effect on the transient response. As $C_{\rm gd}$ is increased, however, the zero moves to a lower frequency where it impacts the frequency and settling time responses of the amplifier. The normalized frequency- and time-domain responses for several values of k_p are shown in Figs. 12 and 13, respectively.

One important drawback of the RHP zero is increased delay in the response of the circuit as $C_{\rm gd}$ is increased. Because $C_{\rm gd}$ scales linearly with the increases in the width needed for higher gain, there is a tradeoff between gain and latency.

TABLE IV
OPTIMAL PEAKING TECHNIQUES

k_C	Desired *BWER*	Desired *STRR* (1%)	Optimal Peaking Method	Parameters for *MST*	Parameters for Flat Amplitude Response
0.1-0.5	< 1.83	< 2.4	Bridged-Shunt	m = 2.84, k_B = 0.1	m = 2.4, k_B = 0.3
0.1-0.4	3-5.59	< 4.1	Asymmetric T-coil	k_C = 0.1, m_1 = 4.1, m_2 = 1.6, k_m = - 0.7 k_C = 0.2, m_1 = 4.6, m_2 = 2.2, k_m = - 0.7 k_C = 0.3, m_1 = 5.0, m_2 = 2.6, k_m = - 0.6	k_C = 0.1, m_1 = 4.0, m_2 = 1.6, k_m = - 0.7 k_C = 0.2, m_1 = 5.5, m_2 = 2.4, k_m = - 0.6 k_C = 0.3, m_1 = 4.0, m_2 = 2.8, k_m = - 0.5
0.4-0.5	3-4	< 1.5	Bridged-Shunt-Series	k_C = 0.4, m_1 = 8.0, m_2 = 2.4, k_B = 0.3	k_C = 0.4, m_1 = 8.0, m_2 = 2.2, k_B = 0.16

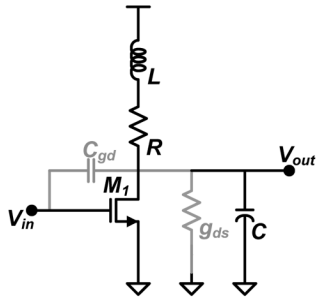

Fig. 11. Shunt-peaked common-source amplifier with nMOS driver device parasitics $C_{\rm gd}$ and $g_{\rm ds}$.

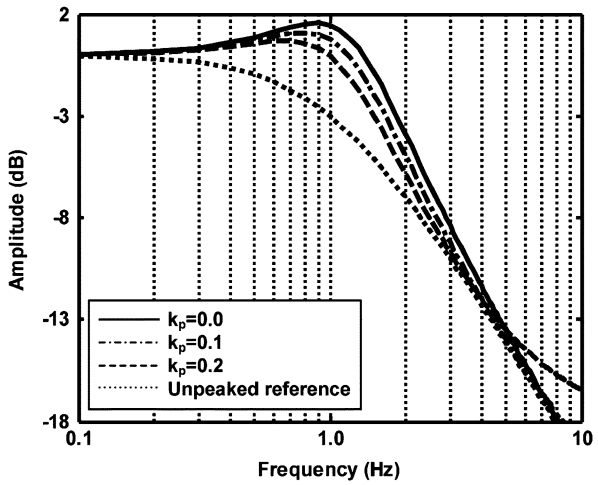

Fig. 12. Normalized frequency-domain magnitude responses of the unpeaked reference amplifier and the shunt-peaked amplifier for several values of $k_p = C_{\rm gd}/(C_{\rm gd}+C)$.

B. Effects of $g_{\rm ds}$

Including $g_{\rm ds}$, the small-signal voltage gain of the shunt-peaked amplifier of Fig. 11 is

$$A_V(s) = -g_m \frac{R+sL}{(1+Rg_{\rm ds})+s(RC+g_{\rm ds}L)+s^2LC}. \tag{10}$$

Substituting $k_r = 1/(1+Rg_{\rm ds})$ and $\omega_g = 1/g_{\rm ds}L$ into (10) gives

$$A_V(s) = -g_m Rk_r \frac{\left(1+\frac{s}{m\omega_0}\right)}{1+\frac{sk_r}{\omega_0}\left(1+\frac{\omega_0}{\omega_g}\right)+\frac{s^2k_r}{m\omega_0^2}}. \tag{11}$$

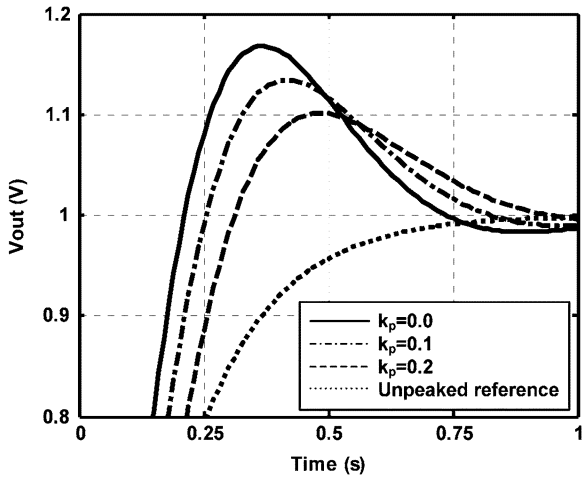

Fig. 13. Normalized time-domain step-responses of the unpeaked reference amplifier and the shunt-peaked design for several values of $k_p = C_{\rm gd}/(C_{\rm gd}+C)$.

From (11), it is clear that finite $g_{\rm ds}$ has two important effects on the response of the circuit. For small $g_{\rm ds}$ (i.e., $k_r = 1$), the response is nearly ideal. However, as $g_{\rm ds}$ is increased, the dc gain is reduced and the complex poles are repositioned. The normalized frequency- and time-domain responses of this system for several values of k_r are shown in Figs. 14 and 15, respectively. It is clear that finite $g_{\rm ds}$ adversely impacts the dc gain of the amplifier as expected (Fig. 14). Because of the paucity of degrees of freedom in the design of a shunt-peaked amplifier, it is difficult to mitigate the effects of the $C_{\rm gd}$ and $g_{\rm ds}$ parasitics without using cascodes; however, other peaking techniques provide more degrees of freedom to exert control over the frequency and transient responses.

The analysis of these parasitic effects is straightforward for the shunt-peaked amplifier; the adverse effects of parasitics are also evident for other peaking techniques, but the increased complexity in the transfer functions obscures intuition. Thus, for more complex peaking techniques such as asymmetric T-coil or bridged-shunt-series, parasitic-aware optimization should be used to optimize the design [15].

IV. DESIGN AND MEASUREMENT RESULTS OF SINGLE-STAGE WIDEBAND AMPLIFIERS

Prototype differential amplifiers employing bridged-shunt-series peaking (Fig. 16(a) with $k_C = 0.4$ and 0.5) and asymmetric T-coil peaking (Fig. 16(b) with $k_C = 0.3$) are designed and fabricated in a 0.18-μm CMOS RF process with six metal layers (top layer thickness $= 2$ μm) [1]. The optimization

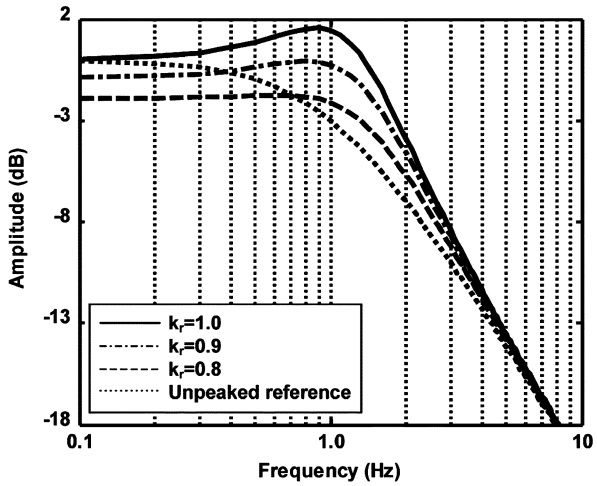

Fig. 14. Normalized frequency-domain magnitude responses of the unpeaked reference amplifier and the shunt-peaked topology for several values of $k_r = 1/(1 + Rg_{\rm ds})$.

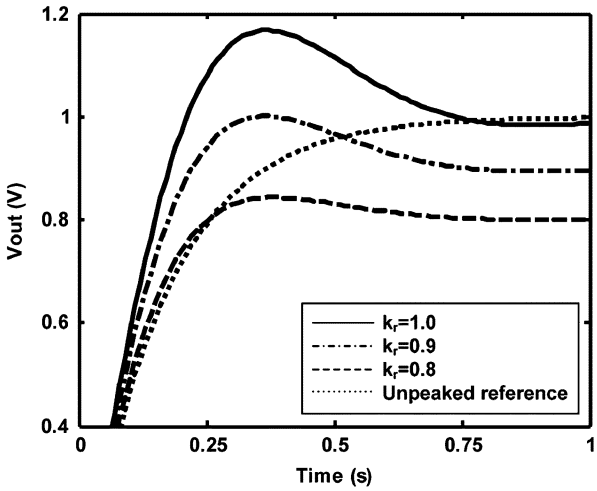

Fig. 15. Normalized time-domain step- responses of the un-peaked reference amplifier and the shunt-peaked amplifier for several values of $k_r = 1/(1 + Rg_{\rm ds})$.

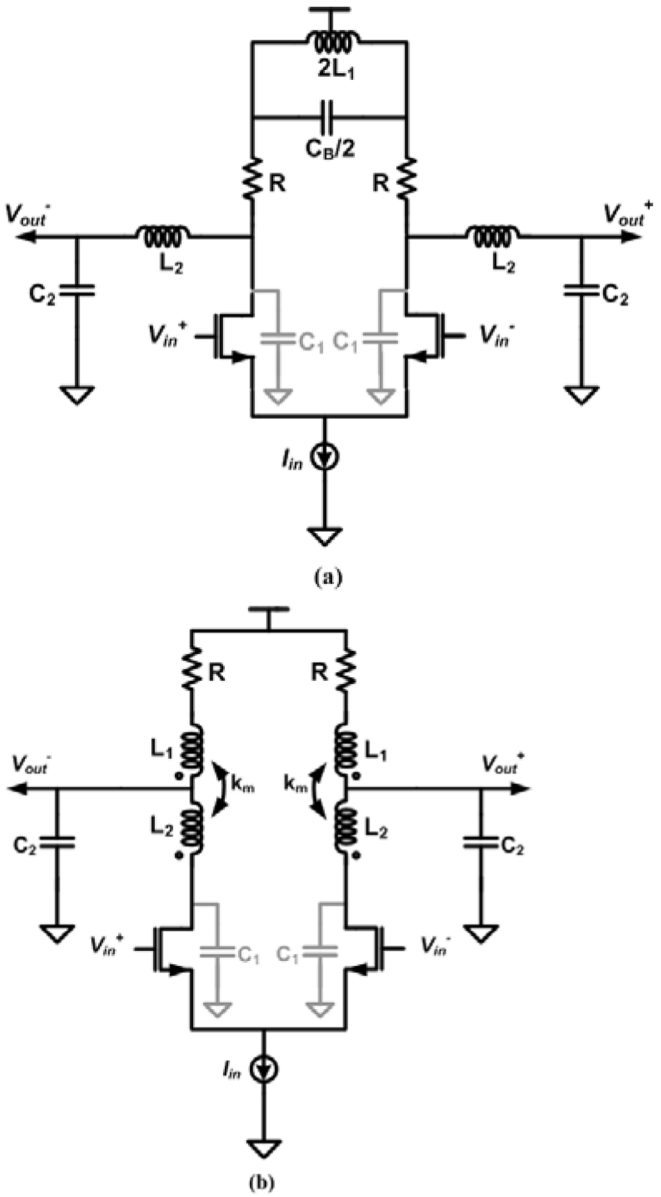

Fig. 16. (a) Bridged-shunt-series-peaked and (b) asymmetric T-coil-peaked differential amplifiers.

objective is high BWER simultaneously with high gain; it necessarily includes accurately modeled passives and routing parasitics as they significantly impact pole-zero placements. In the bridged-shunt-series-peaked amplifiers, a symmetrical center-tapped inductor $(2L_1)$ is used to reduce die area. For $k_C = 0.5$, the required bridging capacitance $(C_B/2)$ is small and realized using the parasitic capacitances of $2L_1$; no explicit C_B is added. In the second bridged-shunt-series-peaked design $(k_C = 0.4)$, $C_B/2$ is realized as a 60-fF MIM capacitor in parallel with the inductor parasitics. For the asymmetric T-coil-peaked amplifier $(k_C = 0.3)$, a T-coil with $k_m = 0.4$ is used [1]. The unpeaked reference amplifiers are also fabricated to facilitate direct comparisons.

The measured voltage gain magnitude and group delay responses extracted from mixed-mode S-parameter measurements are shown in Figs. 17–19(a) and 19(b). The bridged-shunt-series-peaked amplifier with $k_C = 0.4$ exhibits a voltage gain of 14.1 dB, −3-dB BW of 8.0 GHz, BWER of 3.0, and gain peaking of 0.7 dB. The second design with $k_C = 0.5$ shows similar performance except with a gain peaking of 0.3 dB. The asymmetric T-coil-peaked design with $k_C = 0.3$ achieves a gain of 12.1 dB, −3–dB BW of 10.3 GHz, and gain peaking of 1.5 dB. The measured BWER of 4.2 is significantly higher than the best previously reported BWER of 3.5 (theoretical, not measured value). Each differential amplifier draws 15 mA from a 2-V power supply.

The single-stage amplifiers described above are designed to achieve an accurate frequency response. Hence, there are no input and output matching networks, and as a consequence, direct measurement of an eye pattern is not possible. However, the use of measured S-parameter data allows indirect estimates of eye patterns to determine the *relative* maximum data rates that can be transmitted through the various wideband amplifiers. Although the S-parameter measurement does not capture the

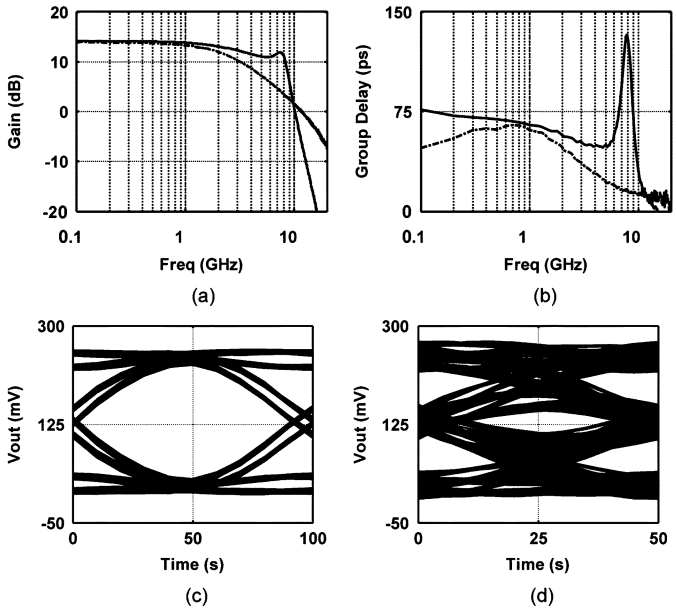

Fig. 17. Measured responses of a bridged-shunt-series peaked amplifier ($k_c = 0.4$) and an unpeaked reference design. (a) Amplitude response and (b) group delay. Pseudo-simulated single-ended output eye diagrams using the measured S-parameters of the amplifiers at data rates of (c) 10 Gb/s and (d) 20 Gb/s with 50-$\mathrm{mV_{PP}}$ input signals.

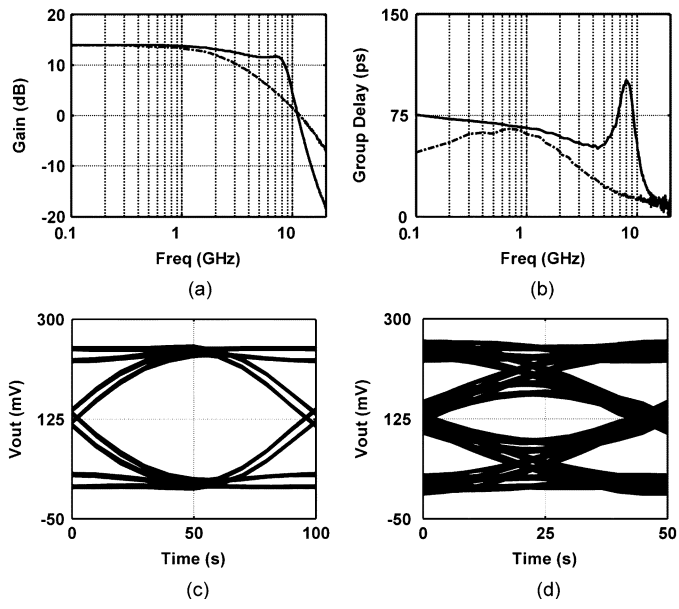

Fig. 18. Measured responses of a bridged-shunt-series peaked amplifier ($k_c = 0.5$) and an unpeaked reference design. (a) Amplitude response and (b) group delay. Pseudo-simulated single-ended output eye diagrams using the measured S-parameters of the amplifiers at data rates of (c) 10 Gb/s and (d) 20 Gb/s with 50-$\mathrm{mV_{PP}}$ input signals.

large-signal behavior of the amplifiers, the relative comparisons are still valid and useful.

To simulate the performance of an amplifier, $2^{16} - 1$ random bits of 50-$\mathrm{mV_{PP}}$ amplitude from a linear feedback shift register (LFSR) are input to a network parameter file as depicted in Fig. 20. The input signal is buffered and split to drive the amplifier under test as well as the unpeaked reference amplifier.

Fig. 19. Measured responses of an asymmetric T-coil peaked amplifier ($k_c = 0.3$) and an unpeaked reference design. (a) Amplitude response and (b) group delay. Pseudo-simulated single-ended output eye-diagrams using the measured S-parameters of the amplifiers at data rates of (c) 10 Gb/s and (d) 20 Gb/s with 50-$\mathrm{mV_{PP}}$ input signals.

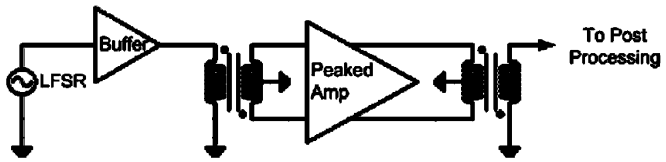

Fig. 20. Setup for the simulation of eye diagrams. Measured S-parameter data of the peaked and unpeaked reference amplifiers is used.

Finally, the outputs are converted from differential to single-ended signals using a balun, and the eye patterns are calculated at the outputs of the network parameter block. As this measurement and simulation does not include the cable losses and reflections, the voltage and timing margin numbers are not precise compared to using a 50-Ω matching network and probing with oscilloscope measurements. However, this approach provides a more accurate estimate than simulations alone, and the *relative* comparisons of different wideband amplifier approaches are still valid.

The pseudo-simulated eye diagrams at 10- and 20-Gb/s data rates for the two bridged-shunt-series-peaked amplifiers and the asymmetric T-coil-peaked design are shown in Figs. 17–19(c) and 19(d), respectively.

V. Design of Multistage Amplifiers

In general, it is desirable to realize the required voltage gain and bandwidth in the fewest stages, which ensures that the overall power dissipation and chip area are minimized [1]. As shown above, it is possible to achieve voltage gain $>$ 10 dB and $-$3-dB BW $>$ 10 GHz in a single wideband amplifier stage in a 0.18-μm CMOS process. However, two system-level

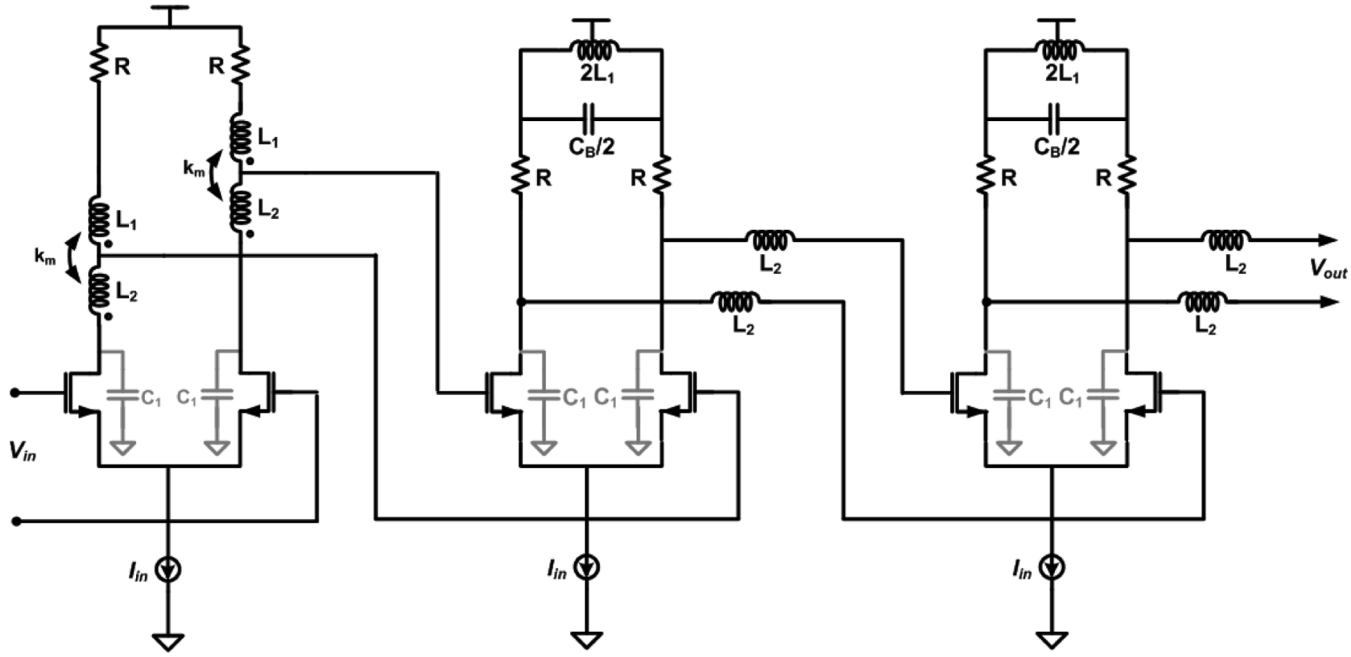

Fig. 21. Three-stage amplifier employing a scaled-up-gain design methodology and optimal peaking technique per stage.

specifications may dictate the use of a multistage cascaded topology—when the bandwidth of the amplifier must be large (a significant fraction of f_T) or when its input capacitance must be small.

1) If the desired bandwidth is large, the voltage gain in each amplifier is traded off against higher bandwidth; hence, several stages must be cascaded to meet the overall gain and BW specifications. A multistage amplifier benefits from the fact that when N *identical* amplifiers with gain A and -3-dB BW ω_0 are cascaded, the overall gain–bandwidth product is increased by the factor $A^{N-1}\sqrt{\sqrt[N]{2}-1}$. Because the overall BW shrinks to $\omega_0\sqrt{\sqrt[N]{2}-1}$, however, each amplifier must have a larger bandwidth than the desired final overall bandwidth. Note that these classical expressions are derived assuming identical amplifiers with no mutual loading effects. If the loading of the next stage is included, and the amplifier is designed so that its individual pole/zero placements are optimized with respect to the response of the next stage, the overall frequency response exhibits much less BW shrinkage. Proper optimization also results in a substantial reduction in gain peaking, even when each individual stage exhibits a relatively high gain peaking. Use of techniques such as staggering may even lead to BW expansion and peaking cancellation [1], [16], [17].
2) Achieving a large gain in a single-stage implies that the stage that drives its input sees a large load capacitance, amplified substantially due to the Miller effect. This may not be allowed in some systems, and, hence, a multistage amplifier design is required to distribute the gain over several stages so that the input driver is not loaded to excess.

For a multistage amplifier design, three basic possibilities exist for the gain distribution: identical gains, scaled-down gains, or scaled-up gains. The first choice, although simple to implement (and thus more popular) because of the identical stages, often requires more stages to meet the gain and BW specifications. Hence, there are power and area penalties and the gain peaking is usually higher. The second choice is optimum for low-noise designs, i.e., it is best suited to applications where the input signal is very small and a high signal-to-noise ratio is required. It is also highly suited to implementations where a small load capacitance is to be driven, and a large input capacitance is permitted [18], [19]. For applications where input capacitance loading is more critical than low-noise performance, the last choice is best: the first stage is designed with the lowest gain, the second stage with a higher gain, and so on.

In cases where a transimpedance gain is needed, a low-impedance common-gate amplifier leads to larger bandwidth compared with a common-source-based design.

This scaled design methodology is used next to demonstrate the design of a high-BW, high-voltage-gain amplifier with low power consumption, realized in three gain stages (Fig. 21) according to the specifications listed in Table V. The f_T of the six-metal 0.18-μm CMOS process is estimated as 47 GHz. In order to ensure small input capacitance, the gain of the first stage is kept small and the gains of the following stages are scaled up. This constrains sizing the transistors in the first stage smaller than the second stage. Given this constraint (smaller k_C) and to obtain maximum bandwidth in the first stage, asymmetric T-coil peaking is utilized. The T-coil modeling is done in the same manner as explained in [1]. The following two high-gain stages employ bridged-shunt-series peaking. A clever gain distribution using *different* types of wideband amplifier stages enables the sizing of the transistors for optimum k_C values for each stage. As a consequence, the desired overall gain and bandwidth specifications are met using fewer stages (e.g., three) than conventional designs that use either identical amplifier stages (e.g.,

TABLE V
SPECIFICATIONS FOR THE MULTISTAGE AMPLIFIER DESIGN

Process	0.18μm CMOS
Maximum Power (mW)	100
Minimum Voltage gain (dB)	12
Data Rate (Gb/s)	40
Load Capacitance (fF)	150

TABLE VI
COMPONENT PARAMETERS AND PERFORMANCE SUMMARY OF EACH INDIVIDUAL STAGE OF THE AMPLIFIER

Stage	Parameters	Gain (dB)	Peaking (dB)	-3dB BW (GHz)
1	R = 51.5Ω L_1 = 505.7pH L_2 = 867pH, k_m = 0.22 W/L = 68.6/0.18	3.2	2.5	23.6
2	R = 51.5Ω $2L_1$ = 260pH L_2 = 447pH C_B = 362.3fF W/L = 90/0.18	4.9	0	23
3	R = 50Ω, $2L_1$ = 142pH L_2 = 408pH C_B = 667fF W/L = 127.4/0.18	7	0	26.9

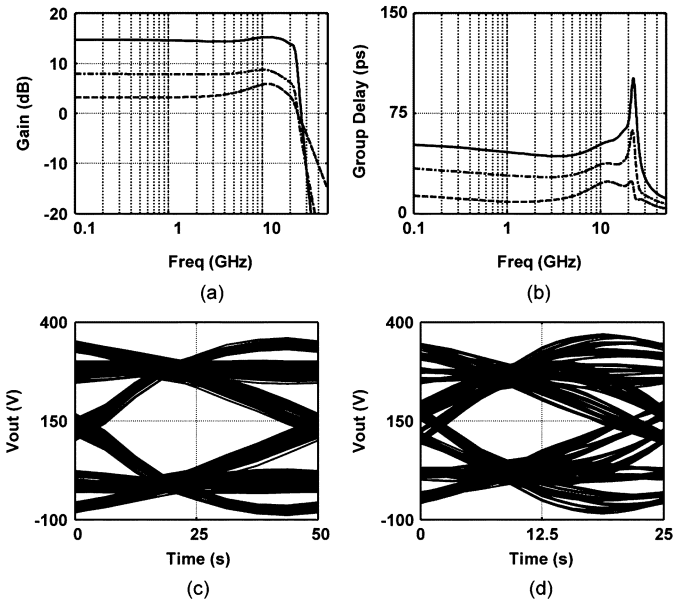

Fig. 22. Multistage amplifier simulated (a) gain and (b) group delay distributions, and single-ended output eye diagrams for data rates of (c) 20 and (d) 40 Gb/s.

five) or stages with identical peaking schemes. The current density in each stage is dictated by its voltage swing, gain and power consumption [14]. After the first pass of the design meets the bandwidth specification, the design is then optimized for a good time-domain response. The values of different components are summarized in Table VI, together with the key frequency-domain characteristics of each individual stage.

Fig. 22 shows the gain and group delay responses for the multistage amplifier. The asymmetric T-coil peaked first stage has a gain of 3.2 dB and a −3-dB bandwidth of 23.6 GHz,

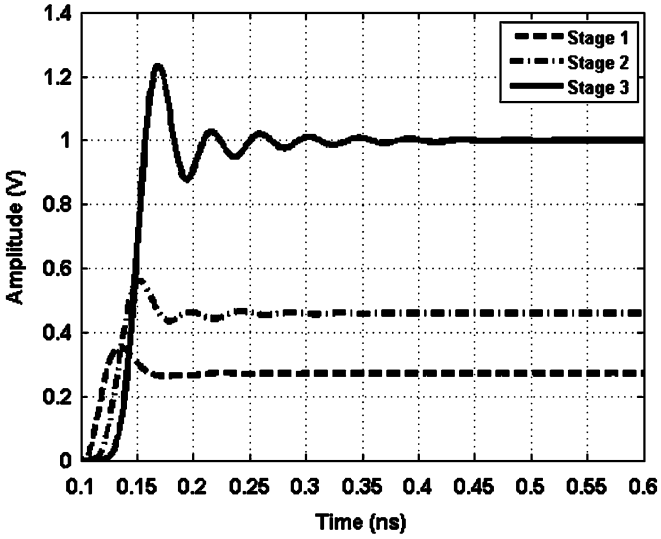

Fig. 23. Multistage amplifier simulated step-responses.

the second bridged-shunt-series-peaked stage ($k_C = 0.5$) has a voltage gain of 4.9 dB and a −3-dB bandwidth of 23 GHz, and the third bridged-shunt-series stage ($k_C = 0.4$) has a gain of 7 dB and bandwidth of 26.9 GHz. The overall amplifier has a gain of 14.7 dB and −3-dB BW of 22.8 GHz. Current consumptions in the three amplifiers are 15.8, 18, and 18.2 mA, respectively, so the total power consumption is 93.6 mW from a 1.8-V supply. By properly optimizing the pole-zero response of each stage, the overall passband peaking is only 0.5 dB even though the individual stages have higher peaking. This peaking compensation is similar to that obtained in gain-staggered distributed amplifiers [16]. The input-referred noise is simulated to be 0.2 $\mathrm{mV_{rms}}$. Fig. 22(c) and (d) shows the simulated eye diagrams at 20 and 40 Gb/s. Finally, the settling performances of each stage are plotted in Fig. 23. After the amplifier is designed primarily for a large bandwidth, a reasonably fast settling time is achieved by making tradeoffs in the amount of peaking in the response. Thus, a scaled-up-gain design methodology combined with different peaking techniques for different stages based on the k_C ratios enables a cascade multistage wideband amplifier design with much less power dissipation and chip area than conventional synthesis approaches that use more stages.

VI. CONCLUSION

Analyses of various bandwidth extension techniques in CMOS wideband amplifiers and a proposed design methodology demonstrate essential tradeoffs among the overall voltage gain, number of gain stages, optimum peaking technique for each stage, rise times, and settling times.

Measured results for several single-stage high-gain amplifiers show that $\mathrm{BWER} > 4$ is achieved, and area and power consumption are minimized.

In cases where single-stage designs are not feasible, a multistage design approach demonstrates that the stages obtain optimal benefit using different peaking techniques as determined by the desired gain distribution, bandwidth, and capacitive loading of the individual stages. Proper design

choices combined with optimization ensure that the multistage amplifier achieves both good bandwidth and settling performance simultaneously with few stages. A three-stage amplifier utilizes a cascade of asymmetric T-coil-peaked and bridged-shunt-series-peaked stages achieves a gain of 14.7 dB with a −3-dB bandwidth of 22.8 GHz with a power consumption of 93.6 mW—performance that exceeds that of conventional multistage designs.

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REFERENCES

[1] S. Shekhar, J. S. Walling, and D. J. Allstot, "Bandwidth extension techniques for CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2424–2439, Nov. 2006.

[2] B. Razavi, *Design of Integrated Circuits for Optical Communications*. New York: McGraw-Hill, 2002.

[3] H. Wheeler, "Wide-band amplifiers for television," *Proc. IRE*, pp. 429–438, Jul. 1939.

[4] F. A. Muller, "High-frequency compensation of *RC* amplifiers," *Proc. IRE*, pp. 1271–1276, Aug. 1954.

[5] B. Hofer, *Amplifier Frequency and Transient Response (AFTR) Notes*. Beaverton, OR: Tektronix, Inc., 1982.

[6] T. H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 1998.

[7] S. Galal and B. Razavi, "40 Gb/s Amplifier and ESD protection circuit in 0.18 μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2389–2396, Dec. 2004.

[8] K. Kanda, D. Yamakazi, T. Yamamoto, M. Horinaka, J. Ogawa, H. Tamura, and H. Onodera, "40 Gb/s 4:1 MUX/1:4 DEMUX in 90 nm standard CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2005, pp. 152–153.

[9] J. Kim, J.-K. Kim, B.-J. Lee, M.-S. Hwang, H.-R. Lee, S.-H. Lee, N. Kim, D.-K. Jeong, and W. Kim, "Circuit techniques for a 40 Gb/s transmitter in 0.13 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2005, pp. 150–151, 589.

[10] H. C. Yang and D. J. Allstot, "Considerations for fast settling operational amplifiers," *IEEE Trans. Circuits Syst.*, vol. 37, no. 3, pp. 326–334, Mar. 1990.

[11] R. C. Dorf and R. H. Bishop, *Modern Control Systems*, 9th ed. Upper Saddle River, NJ: Prentice-Hall, 2001.

[12] A. Worapishet, I. Roopkom, and W. Surakampontorn, "Performance analysis and design of triple-resonance interstage peaking for wideband cascaded CMOS amplifiers," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 54, no. 6, pp. 1189–1203, Jun. 2007.

[13] C. Lee and S.-I. Liu, "A 35-Gb/s limiting amplifier in 0.13 μm CMOS technology," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2006, pp. 122–123.

[14] E. Crain and M. Perrott, "A Numerical design approach for high speed, differential, resistor-loaded, CMOS amplifiers," in *Proc. ISCAS*, Vancouver, BC, Canada, May 2004, pp. 508–511.

[15] D. J. Allstot, K. Choi, and J. Park, *Parasitic-aware Optimization of CMOS RF Circuits*. Norwell, MA: Kluwer, 2003.

[16] D. G. Sarma, "On distributed amplification," *Proc. IRE*, vol. 102B, pp. 689–697, Sep. 1955.

[17] B. Analui and A. Hajimiri, "Multi-pole bandwidth enhancement technique for transimpedance amplifiers," in *Proc. Eur. Solid-State Circuits Conf.*, Sep. 2002, pp. 303–306.

[18] E. Sackinger and W. C. Fischer, "A 3-GHz 32-dB CMOS limiting amplifier for SONET OC-48 receivers," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1884–1888, Dec. 2000.

[19] S. Gondi and B. Razavi, "Equalization and clock and data recovery techniques for 10-Gb/s CMOS serial-link receivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1999–2011, Sep. 2007.

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