A Dual-Polarization Silicon-Photonic Coherent Receiver Front-End Supporting 528 Gb/s/Wavelength

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Abstract—**Supporting advanced modulation schemes such as 16 quadrature-amplitude modulation (QAM) in a high-speed transimpedance amplifier (TIA) requires minimizing noise and total harmonic distortion (THD) across gain settings and frequency. Accordingly, our automatically reconfigurable TIA reduces base resistor noise, gain peaking, phase margin (PM) degradation, and f_T degradation, operating on a single sense voltage and eliminating the need for multiple control loops. A collaborative offset and dc current cancellation technique is introduced to reduce offset-induced nonlinearity, while protecting the receiver (RX) against current overdrive. A prototype of the RX is fabricated on 130-nm SiGe BiCMOS process and demonstrates a maximum gain of 75.5 dBΩ with 35.5 dB of dynamic range, 42-GHz bandwidth (BW), and a maximum gain averaged input-referred noise (IRN) of 18.5 pA/$\sqrt{\text{Hz}}$. The silicon-photonic transceiver assembly incorporating four such RXs achieves 25-dB required optical signal to noise ratio (ROSNR) for received optical power between −22 and 1 dBm at 50 Gbaud, and aggregate data rate of 528 Gb/s/λ at 66 Gbaud and 25-dB ROSNR.**

Index Terms—**Coherent optical communication, dual-polarization (DP), input-referred noise (IRN), receiver (RX), total harmonic distortion (THD), transimpedance amplifier (TIA).**

I. Introduction

COHERENT opto-electronic (O/E) receivers (RXs) support high spectral efficiency through the use of varying-envelope modulation schemes, such as quadrature-amplitude modulation (QAM) and dual-polarization (DP) multiplexing [1], [2], [3]. They require linear transimpedance amplifiers (TIAs) with large transimpedance gain (Z_T) [3], [4], [5], [6], large −3 dB bandwidth (BW) [4], [6], low input-referred noise (IRN) [3], [4], [5], [6], and total harmonic distortion

(THD) [3], [4], [5]. In most of the prior art, efforts were made to reduce IRN when Z_T was at its highest value. Also, linearity improvement was focused at reducing the THD at 1 GHz. From a system point of view, it is valuable to consider higher frequency THD. However, to support data rates beyond 400 Gb/s/λ and complex modulation in links where the RX input signal current (I_{IN}) varies significantly based on the transmitter (TX) power, fiber length, and multiplexing/demultiplexing losses, link considerations demand exceedingly stringent IRN-THD performance: 1) a low THD must be maintained across a large range of I_{IN}; 2) a low THD is important not only at 1 GHz but also up to a frequency of BW/3. For frequencies above that, the third harmonic gets attenuated by the low-pass filtering of the TIA; and 3) IRN should be reduced not only at the maximum Z_T but also at lower Z_T. This is because as the TIA gain is reduced to accommodate a larger I_{IN} and maintain linearity, often the IRN tends to increase in conventional TIA designs. This may even lead to SNR degradation with larger I_{IN} [7] or, at the very least, limit the SNR improvement. Finally, the O/E BW must be sufficiently high to support the data rate, but not exceedingly large, so as to minimize IRN, THD, and channel crosstalk. For example, in our system, to support a 66-Gbaud DP-16QAM operation, a BW of 40–45 GHz proved to be a reasonable target.

In this article, we explain the operation of a coherent RX and explain the motivation behind and the challenges associated with the design of the linear TIAs. Various tradeoffs and techniques necessary to relax those tradeoffs are detailed. We make the following contributions in this work: 1) we present techniques to maintain low THD and low noise across a range of I_{IN}; 2) since RX reconfiguration often becomes challenging, we present an implementation where a single sense voltage is sufficient to automatically reconfigure our TIA across gain settings and frequency; 3) a collaborative offset and dc cancellation circuit operating at the input of the TIA is introduced to reduce offset-induced nonlinearity; and 4) we describe various circuit- and system-level tradeoffs to achieve > 0.5 Tb/s/λ. Other control circuits used in the RX are also described. The rest of this article is organized as follows. A description of operation and requirements for the linear TIA in the context of the DP–QAM silicon-photonic O/E RX is given in Section II. The details of the RX high-speed forward path are presented in Section III. The gain control (GC) as

Fig. 1. DP–QAM silicon-photonic O/E RX.

Fig. 2. Required (a) IRN and (b) THD enhancements (red solid line to green dotted line) to achieve low ROSNR across a wide dynamic range of I_{IN}. (c) Targeted ROSNR performance of the configurable RX.

well as the collaborative offset and dc cancellation circuit are described in Section IV. The test benches used to evaluate the fabricated prototype, along with the experimental results, are summarized in Section V. Finally, conclusion are presented in Section VI.

II. COHERENT SILICON-PHOTONIC RX

Fig. 1 shows a DP–QAM silicon-photonic O/E RX. The received DP optical signal, with a power of P_{RF}, is demultiplexed using a polarization beam splitter and rotator (PBSR) [8], [9]. After demultiplexing the incoming RF signals into X- and Y- polarization, a 90° hybrid is used to down-convert the I- and Q-phase signals directly into baseband, in an intradyne architecture, where the local oscillator (LO) optical frequency is approximately the same as the transmitted frequency ($\omega_{LO} \approx \omega_{RF}$). The details of the 90° hybrid (and the silicon-photonic TX) are described in our prior work [10]. Inside the 90° hybrid, the received signal is split into two paths to be mixed with the LO in the I- and Q-phase fashion. Each photodetector (PD) receives an optical signal $E_{PD}(t) = E_{RF}(t) + E_{LO}(t)$, where $E_{PD}(t)$, $E_{RF}(t)$, and $E_{LO}(t)$ are the electric fields of the incident optical signal on the PD, the received optical signal, and the local laser, respectively. The resulting current I_{PD} follows [3]:

$$I_{PD}(t) = \frac{R}{8}\left(P_{LO} + \sqrt{P_{RF}P_{LO}}\cos\left(\Phi(t)\right)\right) \qquad (1)$$

where R is the PD responsivity (R = 1 A/W in this work), Φ is the phase margin (PM) component of the received signal, and P_{LO} and P_{RF} are the LO power and the received signal power, respectively. As can be seen in the second term of (1), the received input signal experiences an optical gain due to the mixing with P_{LO}. As a result, the sensitivity of the coherent RX is enhanced by increasing the LO power and is superior to that of a direct-detect RX by a factor of $2(P_{LO}/P_{RF})^{1/2}$ [3]. A detailed discussion on the design challenges for a coherent RX is provided in [3]. The high-swing linear output of the RX is digitized and processed via a commercial analog-to-digital converter (ADC) and a coherent digital signal processing (DSP) engine [11], [12], [13], [14], [15].
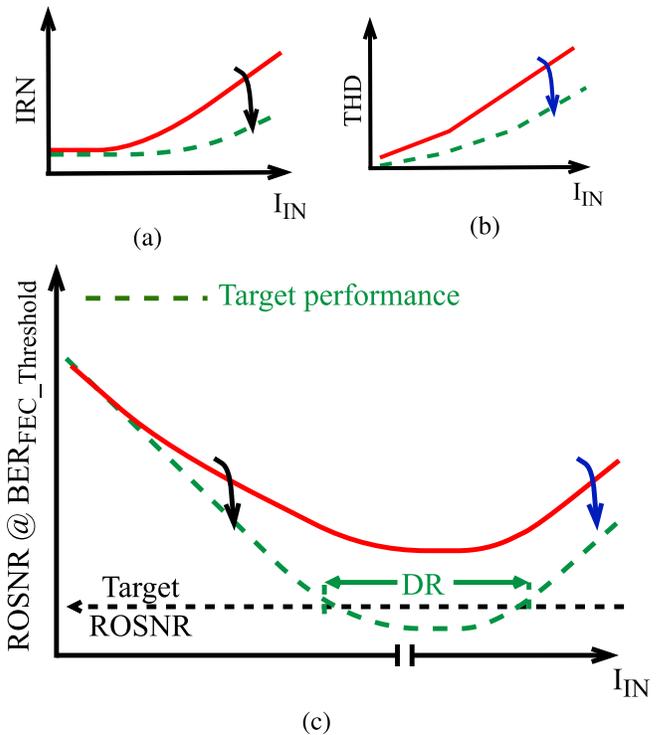
The O/E RX must support a wide range of P_{LO} and P_{RF}, and therefore corresponding I_{IN}, since $I_{IN} \propto P_{RF}$. At very low I_{IN}, the RX is noise-limited and does not meet the required optical signal to noise ratio (ROSNR) target. Recall that a lower ROSNR target at a certain bit error rate (BER) relaxes the TX design and allows for longer reach [16]. Increasing I_{IN} improves the SNR *if the IRN remains constant*. However, to maintain a constant signal swing at the RX output for optimal ADC operation, a larger I_{IN} must accompany an appropriate Z_T reduction. But Z_T reduction usually comes at the expense of a degraded IRN in conventional TIAs [3], [4], [5], [6], as shown by the solid line in Fig. 2(a), limiting the ROSNR improvement and degrading the constellation.

As shown by the solid line in Fig. 2(b), increasing I_{IN} increases the THD for a fixed output swing. Beyond a certain increase in I_{IN}, the RX is pushed in the THD-limited regime, degrading the ROSNR.

Thus, a low target ROSNR for complex modulations such as DP–16QAM constellation, and across a wide range of input signals [Fig. 2(c)], can only be met by making the RX reconfigurable, achieving low noise and THD across gain settings, as shown by the dotted lines in Fig. 2. To realize a wide ROSNR dynamic range, our RX monitors the output level and automatically adjusts the TIA to operate at the optimum point.

III. HIGH-SPEED RX

Fig. 3 shows the block diagram of the RX. The high-speed path consists of a fully differential resistive-feedback TIA,

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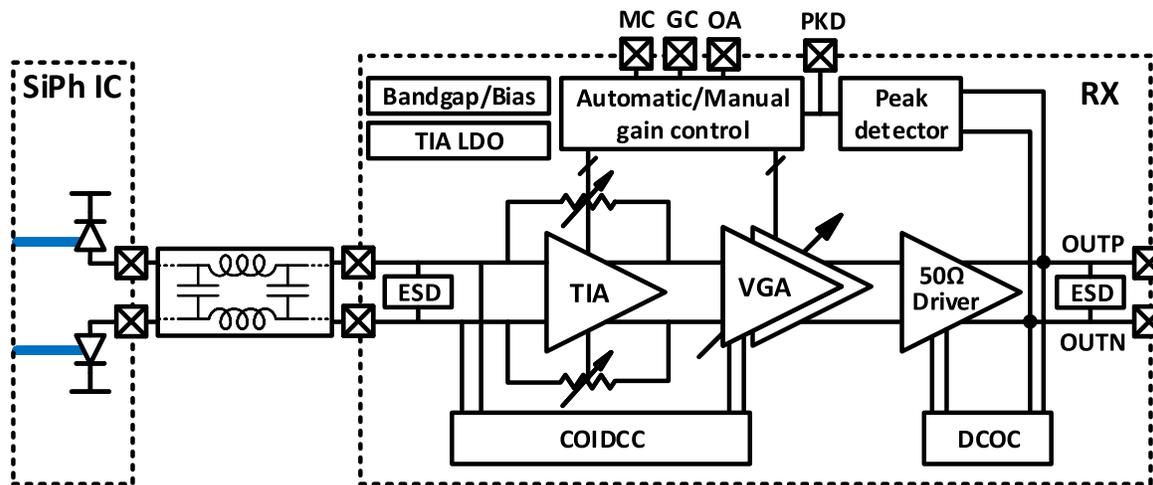
Fig. 3. Block level diagram of a single-channel RX.
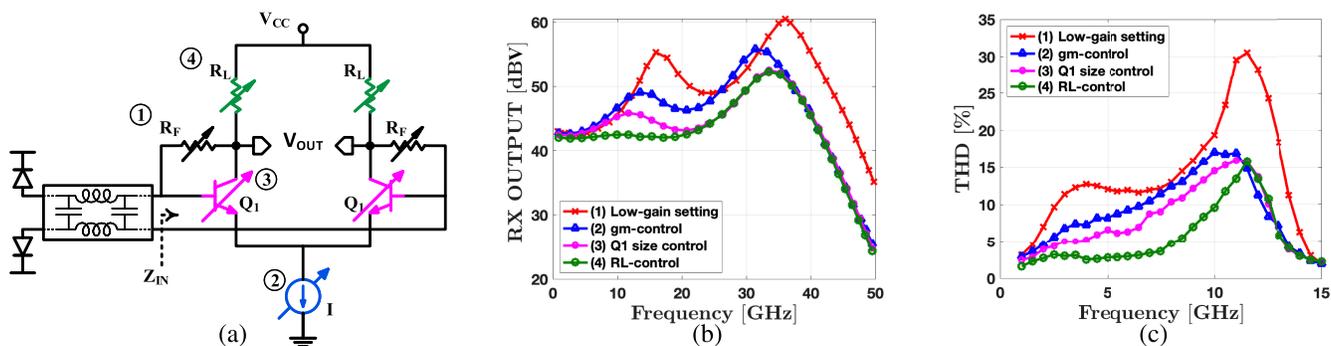
Fig. 4. (a) Simplified schematic for the TIA, and design steps to improve THD across different frequencies for low-gain settings: R_F reconfigurability $\rightarrow$ adding g_m-control $\rightarrow$ adding Q_1 reconfigurability $\rightarrow$ adding R_L-control. (b) Change in the output transfer function along the design steps. (c) Change in the output THD along the design steps. The component parameters' ranges are: R_F = 60–720 Ω, Q_1 = 1–8 μm, I = 1.3–4.3 mA, and R_L = 135–225 Ω.

two current-steering variable gain amplifiers (VGAs), and a 50-Ω output driver. The gain of the TIA and the VGAs can be adjusted manually by an externally applied voltage (GC), or automatically via an automatic GC (AGC) loop. Moreover, a dc offset cancellation (DCOC) loop and a collaborative offset and input dc current (I_{dc}) cancellation (COIDCC) are implemented to protect the RX against mismatches in PDs, TIA, and VGA and against current overdrive. The bandgap [17] provides reference currents to the rest of the RX blocks. A low-dropout regulator (LDO) [18] is used to regulate the 3.3-V supply and provide a 2.8-V supply to the TIA. To protect the RX against electro-static discharge (ESD) events, ESD devices are added to all the pads. The ESD devices provide 500-V protection with $\approx$25-fF capacitance and 2-kV protection with $\approx$95-fF capacitance for the high-speed pads and the dc pads, respectively.

A. Auto-Reconfigurable TIA

The RX first stage is a TIA used to convert the input current from the PDs into a differential voltage. Although a regulated cascode (RGC) TIA [19] promises low input impedance and therefore high BW at low power consumption, its noise performance is inferior to the resistive-feedback TIA [20]. Therefore,

in our design, the first stage is realized using a resistive-feedback TIA. A feedback resistor (R_F) is connected across the input (base) and output (collector) nodes of a differential amplifier, and the TIA gain is approximately R_F [21]. In [4], [5], and [6], the value of R_F, and hence the gain of the first stage, is kept constant. VGAs in subsequent stages realize the dynamic range. However, in long-reach systems where a wide dynamic range is needed, R_F control is also required to realize the low ends of the dynamic range.

Fig. 4 shows the resistive-feedback TIA implemented in our design. To realize the required reconfiguration, a design methodology comprising the following four steps is used.

1) R_F control: R_F control ensures that the low ends of the dynamic range can be realized by reducing R_F. The TIA can be simplified to a two-pole system, one dominant pole at the input at $A_0/(R_F \cdot C_T)$, where A_0 is the forward path gain and C_T is the total input capacitance, and a second pole at the load. When R_F is decreased without changing A_0, the second pole stays constant while the dominant pole frequency increases, so the PM is degraded. This, consequently, leads to unwanted peaking in the output voltage (at 36 GHz in this design) which, in turn, degrades the

Fig. 5. (a) Q_1 reconfigurability for optimizing linearity at large I_{IN} (4 mAppd) and noise at small I_{IN} (100 μAppd). Simulated (b) THD and (c) IRN, comparing a TIA with large (8 μm), small (1 μm), and reconfigurable Q_1.

high-frequency THD, as shown by the curve number (1) in Fig. 4(b) and (c), respectively [21], [22].

As THD is the summation of all the harmonic content (with the third harmonic being the dominant in our design) divided by the fundamental tone, it will be frequency-dependent. The THD calculated from the system's large-signal response can be related to peaking in its small-signal response, with the worst THD at one-third of the peak frequency.

2) g_m control: To enhance the TIA PM, a reduction in R_F is then accompanied by a reduction in the forward path gain. The g_m of Q_1 is reduced by decreasing I_1, and hence the gain of the forward path is reduced. The enhancement in PM due to g_m control maintains a PM > 60° and reduces the gain peaking and the mean of the THD over frequencies up to BW/3 to 9.1%.

However, Q_1 was sized in part to operate near its maximum f_T at the original value of I_1 at high-gain (high R_F) settings. Therefore, at low-gain settings, a reduction in I_1 reduces f_T of Q_1, increases the delay around the feedback loop, and degrades the PM.

3) Q_1 size control: Thus, the g_m control is augmented with Q_1 size control to maintain a high f_T operation across the dynamic range. Note that for an NPN, the impact of Q_1 size control on g_m is not significant. The addition of the Q_1 size control fully uses the benefits of g_m reduction and decreases the mean THD to 7.8%.

4) R_L control: The PD-to-TIA connection acts as an LC network interacting with the TIA's input impedance (Z_{IN}). As R_F changes, Z_{IN} changes and unwanted peaking is created (at 16 GHz in this design) with the most peaking happening at the lowest R_F values. Therefore, in addition to the g_m control, R_L control is introduced to stabilize Z_{IN}, flatten the low-frequency peak, and improve the mean THD to 5.5%.

Moreover, enhancing the PM and reducing the unwanted peaking lowers the group delay variations across gain settings and frequencies up to 30 GHz to less than 30 ps$_{pp}$.

Besides PM enhancement, reconfiguring the size of Q_1 directly impacts the IRN and THD of the RX. At low I_{IN} (high Z_T), RX performance is noise-limited. Given that the parasitic base resistance of Q_1, r_b, acts as a major noise contributor, its value should be minimized by sizing up Q_1 [23]. However, at high I_{IN} (low Z_T), RX performance is THD-limited and the nonlinear parasitic capacitance (C_{bc}) of Q_1 contributes to the high-frequency THD. Thus, sizing Q_1 down improves the high-frequency THD by reducing the impact of the nonlinear C_{bc} [24]. The conflicting requirements for IRN-THD are resolved by splitting Q_1. The effect of splitting was evaluated using simulations to achieve the best performance. As shown in Fig. 5(a), Q_1 is split into Q_{1A} and Q_{1B} with split ratios $\alpha = 0.125$ and $\beta = 0.875$ of the original size A. At low Z_T, the effective size is reduced to Q_{1A} by turning I_2 off. As a result, C_{bc} is reduced lowering the high-frequency THD. As Z_T increases, I_2 starts increasing and Q_{1B} is fully used at maximum TIA gain. As a result, r_b is reduced lowering the IRN. Fig. 5(b) and (c) shows simulated IRN and THD performance comparing a TIA with large, small, and reconfigurable Q_1 devices, respectively. The performance of the reconfigurable device approaches the IRN of the large device at maximum gain, and the THD of the small device at minimum gain, hence covering a wide dynamic range without sacrificing either linearity or noise.

Fig. 6 shows the detailed schematic of the auto-reconfigurable TIA. In this design, a coarse tuning for Q_1 is implemented by splitting Q_1 into Q_{1A} and Q_{1B}. Q_{1A} is always on, while Q_{1B} is turned on at low input currents to minimize the noise contribution of Q_1. $g_{m\text{-CTRL}}$ input current is used to control Q_1 while controlling the overall transconductance of the forward path (G_m). A variable feedback resistor is realized by connecting an n-channel field effect transistor (NFET) device (N_1) operating in the linear region in parallel with R_F and controlled via $R_{F\text{-CTRL}}$. A variable load resistor is realized by splitting R_L into two resistors in series, and a p-channel field effect transistor (PFET) device (P_1) is used to control the effective value of the load. To shield the TIA loop from VGA loading, a separate emitter follower (Q_4) is used as the output stage of the TIA.

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Fig. 6. Detailed schematic for the auto-reconfigurable TIA.

Due to the dynamic changes in g_m and R_L, the common-mode voltages in the TIA loop and at the TIA output can experience large variations potentially putting the RX at suboptimal bias points. To compensate for the common-mode changes, $R_{DC1,2}$ ($\approx$2.3 kΩ) are thus augmented into the TIA and the IR drops on them are varied via $I_{DC1,2}$. $C_{DC1,2}$ ($\approx$230 fF) are used to minimize any effect this technique might have on the small-signal response. The values of $I_{DC1,2}$ are linked to $g_{m\text{-CTRL}}$ and $R_{L\text{-CTRL}}$ across different gain settings to maintain constant common modes.

Since each of the aforementioned control signals is dependent on the gain, they can be generated by processing the GC voltage generated in the AGC loop as discussed in Section IV-A.

B. Variable Gain Amplifier

Two VGAs, with a schematic as shown in Fig. 7, are used to extend the gain range beyond the TIA maximum gain. The gain of the VGA is varied by controlling ($Q_3 - Q_6$) to steer the signal current between the load (R_L) and the supply (V_{CC}). Such a structure is favored over the classical Gilbert cell as a VGA since it achieves better BW across the dynamic range [3], [5] and better IRN at low gain [25]. Series-shunt inductive (L_1, L_2) peaking is used to extend the BW of the VGAs by 1.22$\times$ (at the maximum gain setting of the VGA) to achieve the targeted BW [26], [27]. Even though the same inductive peaking is used for all the gain settings, lower gains show more peaking due to PM reduction in the TIA loop. Moreover, a degeneration resistance (R_E) is used to enhance the VGA linearity [3], and a variable capacitance (C_E) is used to introduce a gain-dependent continuous time linear equalization (CTLE) [28] to enhance the BW at high-gain operation without adding unwanted peaking at the low-gain operation. Since both the peaking mechanisms also impact the THD and group delay, only limited peaking was used
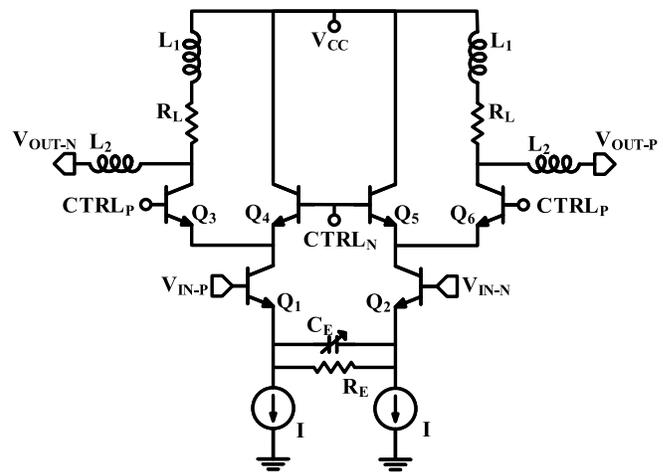
Fig. 7. Circuit schematic for the VGA with shunt-series peaking and CTLE.

to maintain the THD and group delay within the targeted specifications.

IV. LOW-SPEED FEEDBACK PATH

A. Gain Control

The gain of the TIA and the VGAs can be adjusted manually by an externally applied GC voltage, or automatically via an automatic GC loop. As shown in Fig. 8, in the AGC mode, the output level (V_{DRV}) is estimated by a peak detector (PKD) circuit [29] and compared with an externally applied voltage set to get a target output amplitude (OA). The result of comparing V_{OA} to the PKD output is the GC voltage (V_{GC}). A comparator with RC filtering and a Miller-amplified C_{PKD} is used to compare V_{OA} and V_{PKD}. The AGC must be slower than the minimum frequency the data contains to avoid distorting the signal. To ensure that, the PKD and selector are designed
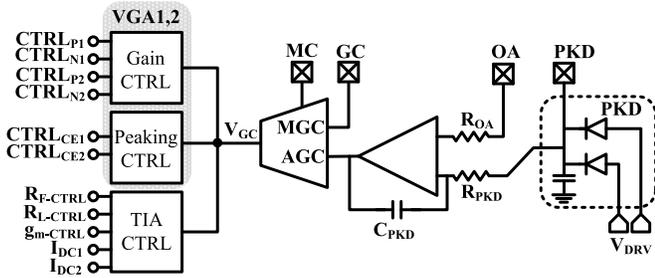
Fig. 8. Block diagram of the GC system.
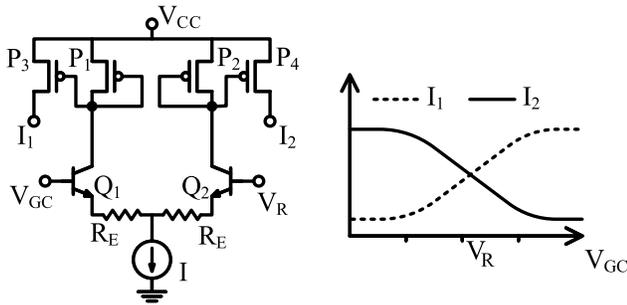
Fig. 9. Building block for generating various control signals.

Fig. 10. Representation of the main control signals. Showing the change in R_F, R_L, and g_m of the TIA, and the gains of VGA1 and VGA2 versus V_{GC}.

Fig. 11. Different options for DCOC correction.

to have a high-frequency cutoff of several MHz, while the comparator has a unity gain frequency below 1 MHz. Then, when the loop is closed, the AGC maximum frequency of operation is below 1 MHz. Alternatively, in manual mode, V_{GC} can be applied externally and the AGC loop is broken. An analog multiplexer with an externally applied mode control (MC) signal is used to select between manual GC (MGC) and automatic GC (AGC). In both the cases, V_{GC} is then processed in the control generation blocks and TIA/VGA control signals are generated.

To generate the control signals, V_{GC} is fed into multiple control generation circuits, whose building block is shown in Fig. 9. The building block consists of a differential amplifier (Q_1 and Q_2) with diode-connected loads and current mirrors ($P_1 - P_4$) acting as controlled current sources. Fig. 9 also shows the controlled currents, I_1 and I_2, as a function of V_{GC}. The curves resemble the dc transfer characteristics of a differential amplifier following a hyperbolic tangent function. The reference voltage (V_R), which is generated ON-chip, is used to control the threshold of change for I_1 and I_2 and shift their curves on the V_{GC} axis. Meanwhile, the tail current (I) is used to control the dynamic range of I_1 and I_2 (and hence the dynamic range of the control signal). Finally, the degeneration resistance (R_E) is used to control I_1 and I_2's slope (linearity) versus V_{GC}. To generate the control signal ON-chip for the TIA/VGAs, V_R, I, and R_E are chosen uniquely so as to eliminate the need for look-up tables. The control currents are fed to high-speed blocks where they are converted into control voltages.

Fig. 10 shows the main control signals for the TIA and the VGAs versus the GC voltage V_{GC}. R_F is varied by controlling a shunt NFET, while R_L is varied by controlling a shunt PFET, and g_m is varied by controlling the tail current, as discussed in Section III-A and shown in Fig. 6. At high
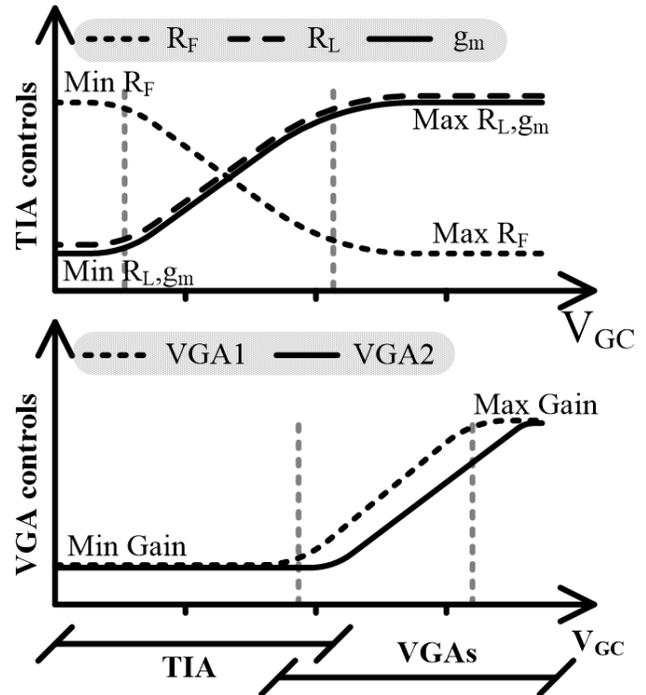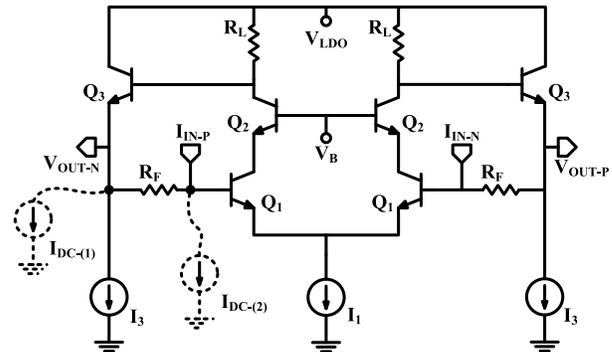
input currents (low V_{GC}), R_F is minimized by turning the shunt NFET on, while R_L and g_m are also minimized to meet the required performance as discussed in Section III-A. As the input signal reduces (V_{GC} increases), R_F along with R_L and g_m are increased to reach their maximum values. To get the best noise performance across the dynamic range, the gain stages are sequentially controlled. The TIA gain is maximized first, and then the VGAs start contributing to Z_T with VGA1 starting slightly before VGA2 ($V_{R,\mathrm{VGA1}} < V_{R,\mathrm{VGA2}}$). This permits the RX to benefit from any increase in the input signal without significantly increasing the RX noise contribution, hence enhancing the SNR.

B. Collaborative Offset and DC Cancellation

In a coherent O/E RX, the received signal is mixed with the LO and then applied to the PD. Consequently, an increase in the LO power increases the input current to the TIA

Fig. 12. Collaborative offset and IDCC.

and enhances the RX sensitivity. However, it also increases the PD I_{dc} as a mixing side product. Thus, I_{dc} cancellation (IDCC) loop is essential for each input to retain enhanced sensitivity and protect the RX from current overdrive [3], [4]. In addition, a DCOC loop is required to cancel any offset in the TIA or between the two IDCCs. The DCOC senses the difference between P and N of a differential signal at its input and corrects the offset by drawing unbalanced current at its output. The output of the DCOC can be connected to either the input or the output of the TIA, as shown in Fig. 11. In [3], the DCOC is connected to the TIA output and annotated in Fig. 11 as $I_{DC(1)}$. In this configuration, the DCOC load is an emitter-follower stage dropping the DCOC gain significantly and limiting its correction range. The correction voltage (ΔV_{DC}) changes logarithmically with $I_{DC(1)}$ as shown in the following equation:

$$\Delta V_{dc} = \frac{V_T}{\ln(I_s)} \ln\left(\frac{I_3 + I_{dc-(1)}}{I_3}\right) \quad (2)$$

where V_T is the thermal voltage of the junction, I_s is the saturation current, and I_3 is the emitter-follower bias current. Moreover, any offset from the PDs and/or the IDCCs will propagate through the TIA degrading dynamic performance including THD. Therefore, a better approach is to correct the TIA offset at its input as annotated on Fig. 11 by $I_{DC(2)}$. In this configuration, ΔV_{DC} has a stronger dependence on $I_{DC(2)}$ and can be corrected more efficiently as shown by the following equation:

$$\Delta V_{dc} = R_F I_{DC(2)} + \frac{V_T}{\ln(I_s)} \ln\left(\frac{I_3 + I_{DC(2)}}{I_3}\right) \quad (3)$$

where R_F is the TIA shunt-feedback resistor. However, in the proposed configuration, both IDCC and DCOC attempting to set input CM voltages can create contention. Thus, a collaborative offset and IDCC (COIDCC) loop is proposed, as shown in Fig. 12. In the proposed COIDCC, a DCOC is used to compare the common modes at the emitters of the input differential pair of the VGA (Q_1 and Q_2 in Fig. 7) and sense for dc offset. Then, a reference generation (REF GEN) block is used

to generate the references for the IDCC (V_{R-P} and V_{R-N}). In the REF GEN, and when $V_{DCOC} = V_R$, the tail current I is divided into half between Q_P and Q_N, and the reference voltages follow:

$$V_{R-P/N} = V_{BE-P/N} + R_{R-P/N}\left(I_{R-P/N} - \frac{I}{2}\right) \quad (4)$$

where $V_{BE-P/N}$ is the base–emitter voltage of $Q_{P/N}$, and $I_{R-P/N}$ are the reference currents from the bandgap. In the presence of a dc offset, the tail current I is divided unevenly, and new customized references are generated for the IDCC. Hence, the COIDCC protects the first stage against high I_{dc} and resolves offset at the very input to maintain high linearity.

To evaluate the COIDCC performance, dc and time-domain simulations have been performed. Mismatched dc currents were injected to P (2 mA) and N (1 mA) terminals, kept constant, and then removed. The effect of this process was evaluated in a time-domain simulation while monitoring the input and output voltages as shown in Fig. 13(a) and (b). The figure shows the single-ended inputs and outputs of the RX. The COIDCC was able to maintain proper dc levels to the introduced events at 10 and 40 ns. To evaluate the effect of process variations in the output offset, Monte Carlo simulations were performed with the COIDCC enabled and disabled. Fig. 13(c) shows the loop effect in canceling the offset introduced by process variations. With the loop turned off, the output offset can reach ± 180 mV. With the loop turned on, the output offset is limited to ± 6 mV.

V. MEASUREMENT RESULTS

A prototype 2-channel RX chip is fabricated on a 250-GHz-f_T 130-nm SiGe BiCMOS process. Two 2-channel RX dies and a SiPh chip are flip-chipped using copper pillars to a ceramic ball grid array (BGA) substrate and co-packaged, as shown in Fig. 14. The full assembly of the coherent transceiver is tested at 1550 nm similar to our prior work [30].

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(a)

(b)

(C)

Fig. 13.   (a) TIA single-ended input voltages. (b) TIA single-ended output voltages. (c) Monte Carlo simulations with the COIDCC enabled and disabled.

(a)

(b)

Fig. 14.   (a) Die micrographs depicting the O/E RX: silicon-photonic IC along with 2x2 RX ICs, and a zoom-in view on the RX IC. (b) Flip-chipped assembly on a ceramic BGA.
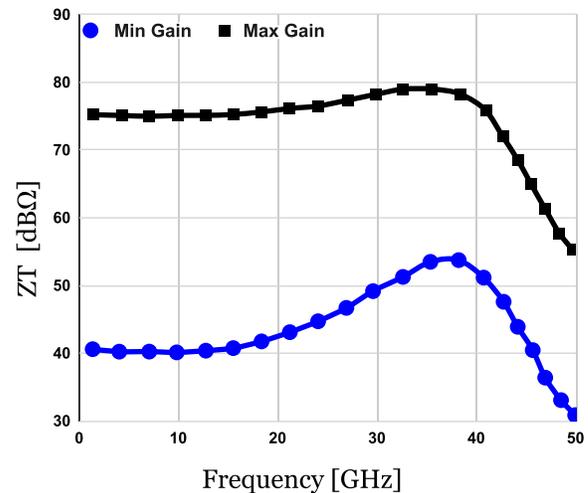
Fig. 15.   Measured Z_T versus frequency, with the maximum and minimum gain curves shown.

First, the electrical RX is tested on-wafer, in a 50 Ω environment without other loading effects (such as packaging), using a 50-GHz vector network analyzer (VNA) with a smoothing filter enabled. The measured differential S-parameters are used to calculate the electrical RX Z_T as in the following equation:

$$Z_T(f) = Z_o \frac{S_{21}(f)}{1 - S_{11}(f)} \tag{5}$$

where Z_o is the port impedance, which is 50 Ω for the VNA.

Fig. 15 shows the measured Z_T at maximum and minimum gain settings. Z_T reaches a maximum of 75.5 dBΩ and covers a range of 35.5 dB while maintaining a BW > 40 GHz across gain settings. Since the same peaking techniques are used for all the gain settings, the difference in peaking can be attributed to the TIA, which is made much better, thanks to the proposed techniques. The small discrepancy between the measured and simulated peaking locations can be attributed to the discrepancy between postlayout simulations and the actual silicon performance. Fig. 16 shows

the measured group delay at minimum and maximum gain settings. The group delay variations up to 30 GHz are less than 30 ps$_{pp}$.

The VNA is also used to measure the RX THD at different frequencies and up to 4 mAppd of the input current , and for an output voltage of 500 mVppd, as shown in Fig. 17. The THD at 1 GHz remains low across the range of input current, and the worst measured THD at 10 GHz is still below 10%, with an average THD of 4.4% at 3 mAppd.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON TO PRIOR ART

	This work	[3]	[4]	[5]	[6]	[7]	[31]	[32]
Baud rate (Gbaud)	66	34	64	32/25	100/50	56/50	53	64
Modulation	DP-16QAM	DP-16QAM	SP-QPSK	NRZ/PAM-4	NRZ/PAM-4	NRZ/PAM-4	PAM-4	PAM-4
O/E RX bit rate (Gb/s)	528	272	128	32/50	100	112/100	106.25	128
–3dB Elec. BW (GHz)	42	27	53	33	42	65	27	45.5
Max Z_T (dBΩ)	75.5	73	80	74	68.5	71	78	59.3
Z_T range (dB)	35.5	43	34	24	20	10	21	-
Target ROSNR[1] (dB)	25	N/R						
BER	1E-2	5.4E-4	9E-6	<1E-10	N/R	N/R	1E-16	2.4E-4
IRN @ max Z_T (pA/$\sqrt{Hz}$)	18.5	20	24.8	12.2	8	7.2	16.7	12.6
IRN @ 500Ω (pA/$\sqrt{Hz}$)	42	100	65	40	N/R			
1GHz THD @0.5mAppd (%)	0.6[2]	1.1[2]	0.6[3]	0.8[3]	N/R	1.3[2]	1.4[3]	11[4]
1GHz THD @3mAppd (%)	2.2[2]	N/R	2.55[3]	N/R				
Avg.[5] THD @3mAppd (%)	4.4	N/R						
Supply voltage (V)	3.3	3.3	3.3	3.3	3.3	3.3	1.8	0.8
Power/TIA (mW)	275	313	277	218	150	345	60.8	11.2
Technology	130nm SiGe						16nm FinFET	22nm FinFET

[1]50Gbaud DP-16QAM, [2]500mVppd output, [3]600mVppd output, [4]460mVppd output, [5]Averaged over frequency
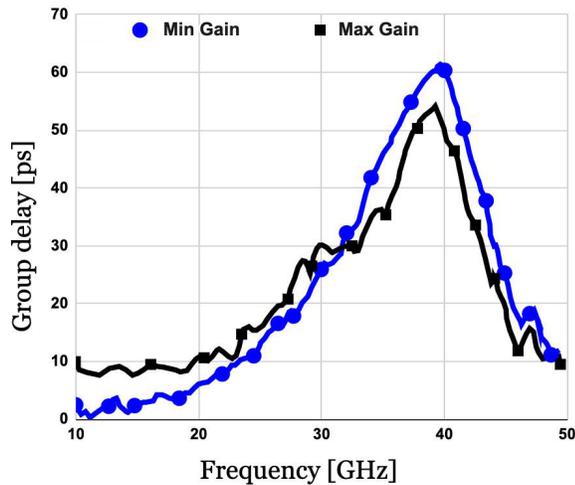
Fig. 16. Measured group delay versus frequency, with the maximum and minimum gain curves shown.

Fig. 17. Measured THD at different frequencies and inputs.

A spectrum analyzer is used to measure the RX noise. The output of the TIA is connected to a spectrum analyzer as the inputs are kept floating. The increase in the noise power from the noise floor is then used to calculate the TIA-added noise, and Fig. 18 shows the measured IRN versus Z_T. The TIA achieves an IRN of 18.5 pA/$\sqrt{Hz}$ at the maximum gain. The simulated IRN at maximum gain is dominated by the input pair base resistance at 31% contribution, the input pair shot noise at 17%, the emitter followers in the TIA at 6.5%, the input pair emitter resistance at 5.5%, and R_F at 4.5%. Moreover, the degradation in IRN as the gain drops to 500 Ω is small in our reconfigurable TIA, allowing the SNR to benefit from any received signal increase.

Thanks to the COIDCC, the TIA can handle up to 8.5 mA of the measured I_{dc} into each terminal, as shown in Fig. 19. Beyond 8.5 mA, the COIDCC cannot cancel all I_{dc}. The excess current flows into the TIA and causes the input common mode to change deviating from the reference voltage.

Fig. 18. Measured IRN versus Z_T.

Finally, the ROSNR of the complete O/E RX is tested. Our prior work on TX [10] discusses ROSNR, and its

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

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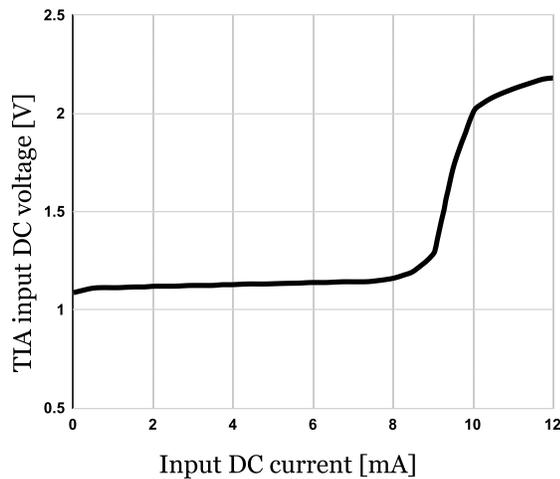
Fig. 19.   Measured input dc voltage versus injected dc current.
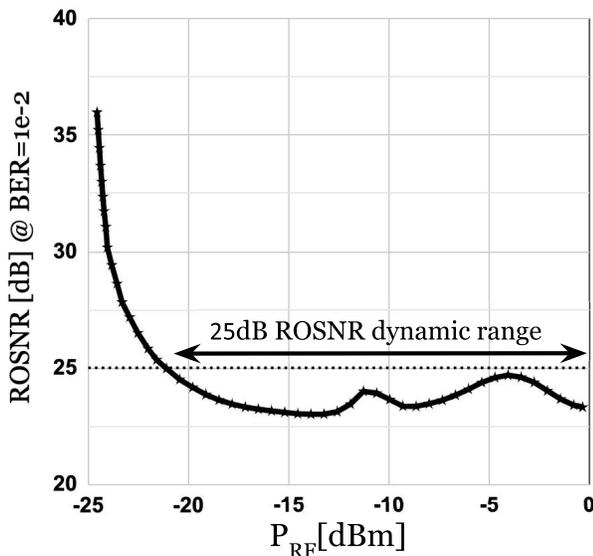
Fig. 20.   Measured 50-Gbaud DP–16QAM ROSNR at BER = 1E-2.
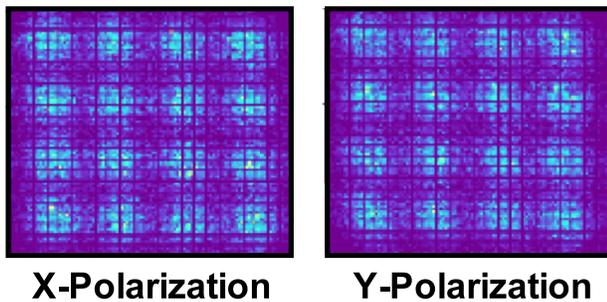
Fig. 21.   Measured constellations for 528 Gb/s DP–16QAM O/E RX.

calculation and measurement methods. Fig. 20 shows the ROSNR measurements at 50-Gbaud DP–16QAM with varying input at the RX. Thanks to the auto-reconfigurable TIA, the O/E RX meets the target 25-dB ROSNR at 400 Gb/s/λ for P_{RF} within the range of –22 to 1 dBm (limited by test setup) at the commercial DSP forward error correction (FEC) threshold of 1E-2 allowing for zero post-FEC errors. The system, including
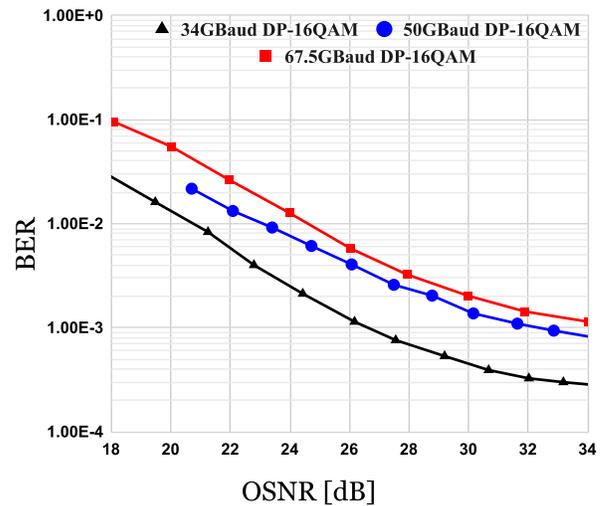
Fig. 22.   Measured BER versus OSNR at different data rates and modulation formats.

the DSP filtering and equalization, was used to measure the constellation right at the FEC threshold (BER = 1E-2). Fig. 21 shows the pre-FEC constellations for 66-Gbaud DP–16QAM, achieving 528 Gb/s per wavelength with zero post-FEC errors. The BER versus optical signal to noise ratio (OSNR) was also measured at different data rates and modulation formats as shown in Fig. 22.

Table I summarizes the performance and compares it to prior art. The O/E RX achieves the highest aggregate bit rate using DP–16QAM modulation. Moreover, the proposed RX achieves low IRN at maximum gain and at 500 Ω, while maintaining the average THD over frequencies under 5% and up to 3 mAppd. By optimizing for noise and linearity, the O/E RX achieves the targeted ROSNR across a wide dynamic range.

VI. Conclusion

In this article, we present a silicon-photonic-based coherent O/E RX. The spectral efficiency of the O/E RX is enhanced using advanced modulations, such as QPSK and QAM, and polarization demultiplexing. Our RX relies on an auto-reconfigurable TIA that minimizes THD and noise across a wide range of input signal and frequencies. The O/E RX meets the target ROSNR across a wide range of input signal. To the best of our knowledge, this is the first published work to report an auto-reconfigurable TIA relaxing the IRN-THD tradeoff, focused on minimizing the high-frequency THD and supporting > 0.5 Tb/s/λ DP–16QAM.

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